SRI SRINIVASA EDUCATIONAL & CHARITABLE TRUST (R)

Sapthagiri College of Engineering

(Affiliated to Visvesvaraya Technological University, Belgaum & Approved by AICTE, New Delhi)

STUDENTS FEEDBACK ON CURRICULUM

This questionnaire is to collect information relating to your satisfaction towards curriculum for creating conducive atmosphere for teaching and learning. The information provided by you will be kept confidential and will be used as important feedback for quality improvement of the program of studies/institution.

Academic Year	2015-2016
Branch	Electronics and communication Engineering
Name of the Student	Lavanya.P
USN	1SG16EC048

Rate the curriculum/syllabus on the following Points

SL NO	Statements	Excellent	Very good	Good	Average	Below Average
		5	4	3	2	1
1	How do you rate the syllabus of the courses that you have studied in relation to the competencies expected out of the course?	✓				
2	How do you rate the allocation of the credits to the courses?		✓			
3	Relevance for implementation in projects			✓		
4	How do you rate the electives offered in relation to the technolcgical advancements?	✓				
5	How do rate the evaluation scheme designed for each of the course?				✓	
6	How do you rate the percentage of courses having LAB components?	✓				
7	Curriculum is sufficient to make you analyze the engineering problems and its suitable solution			✓		
8	Suggestions (if any)	I suggest to have more programs to check LVS, DRC & ORC of the IC's				

Suggestions: Overall, the lab was a good exposure for us regarding the design of chips, verification of the IC design flow etc. but I suggest to have more programs in designing to check LVS, DRC & DRC of the IC's

Signature

Lavanyap

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Bengaluru - 560 057

Principal
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Bengaluru - 560 057

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STUDENTS FEEDBACK ON CURRICULUM

This questionnaire is to collect information relating to your satisfaction towards curriculum for creating conducive atmosphere for teaching and learning. The information provided by you will be kept confidential and will be used as important feedback for quality improvement of the program of studies/institution.

Academic Year	2018-2019
Branch	Electronics and Communication
Name of the Student	Nayana T.R
USN	1SG16EC062

Rate the curriculum/syllabus on the following Points

SL NO	Statements	Excellent	Very good	Good	Average	Below Average
		5	4	3	2	1
1	How do you rate the syllabus of the courses that you have studied in relation to the competencies expected out of the course?	✓				
2	How do you rate the allocation of the credits to the courses?			✓		
3	Relevance for implementation in projects		✓			
4	How do you rate the electives offered in relation to the technological advancements?				✓	
5	How do rate the evaluation scheme designed for each of the course?		✓			
6	How do you rate the percentage of courses having LAB components?			✓		
7	Curriculum is sufficient to make you analyze the engineering problems and its suitable solution	✓				
8	Suggestions (if any)	Number of hours should be increased because, the programs ~~are~~ consume much more time.				

Suggestions:

- As I am know theory, practical Labs provide me to gain more knowledge about working industry

Signature

Nayana

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STUDENTS FEEDBACK ON CURRICULUM

This questionnaire is to collect information relating to your satisfaction towards curriculum for creating conducive atmosphere for teaching and learning. The information provided by you will be kept confidential and will be used as important feedback for quality improvement of the program of studies/institution.

Academic Year	2015 - 16
Branch	Electronic And Communication
Name of the Student	H.N. Bhavana Jain
USN	1SG13EC032

Rate the curriculum/syl abus on the following Points

SL NO	Statements	Excellent	Very good	Good	Average	Below Average
		5	4	3	2	1
1	How do you rate the syl abus of the courses that you have studied in relation to the competencies expected out of the course?		✓			
2	How do you rate the allocation of the credits to the courses?		✓			
3	Relevance for implementation in projects	✓				
4	How do you rate the electives offered in relation to the technological advancements?	✓				
5	How do rate the evaluation scheme designed for each of the course?		✓			
6	How do you rate the percentage of courses having LAB components?	✓				
7	Curriculum is sufficient to make you analyze the engineering problems and its suitable solution		✓			
8	Suggestions (if any)					

Suggestions: → Prescribe to syallbus needs to maintain industrial standards.

Bhavana H.N.
Signature → There is much gap between industrial requirement & syallbus

→ FPGA design environment is very brief.

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FACULTY FEEDBACK ON CURRICULUM

This questionnaire is intended to collect information relating to your satisfaction towards the curriculum, teaching, learning and evaluation. The information provided by you will be kept confidential and will be used as important feedback for quality improvement of the program of studies/institution.

Academic Year	2015-16
Branch	ECE
Name of the Faculty	SHOBHA H.
Designation	Asst Prof
Subject/Sub. code	Fundamentals of CMOS VLSI (10EC56)

Rate the curriculum/syllabus on the following Points

SL NO	Statements	Excellent	Very good	Good	Average	Below Average
		5	4	3	2	1
1	Do you feel that the curriculum is defined in a way to clarify your teaching goals and what you expect your students to learn?	✓				
2	Is the curriculum suffcient to bridge the gap between industry standards ,current global scenarios and academics?			✓		
3	Is the timely coverage of curriculum possible in the mentioned number of hours?		✓			
4	Suffcient reference material and books are available for the topics mentioned in the curriculum?	✓				
5	The evaluation methods mentioned in the curriculum are suffcient for providing proper assessment?		✓			
6	Curriculum is suitable to the course		✓			
7	The curriculum/course of this subject increased my knowledge and perspective in the subject area			✓		

Suggestions: * To meet industry requirement in area of VLSI design, certification course is required for students.

Signature

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ALUMNI FEEDBACK ON CURRICULUM

We are glad that you have spent valuable years pursuing courses of your choice at SCE. We shall be thankful if you can spare some of your valuable time to fill up this feedback form and give us valuable suggestions for further improvement of the College. Your valuable inputs will be of great use to improve the quality of our academic programs and enhance the credibility of our Institution. Rate the adequacy of following as they were during your tenure as a student

Year of Passing	2012
Branch	ECE
Name	T V Swaroop
Status : Work/Study	Work INTEL
Phone no.	8105024241

Rate the curriculum/syllabus on the following Points

SL NO	Statements	Excellent	Very good	Good	Average	Below Average
		5	4	3	2	1
1	When you compare yourself with other counterparts from other Institution, you feel that you got most of all the facilities which is not available in other Institution			✓		
2	Learning value (in terms of skills, concepts, knowledge, analytical abilities or broadening perspectives)				✓	
3	Curriculum is sufficient to make you analyze the engineering problems and its suitable solution				✓	
4	How do you rate the learning experience in terms of their relevance to the real life application				✓	
5	Ability to work in teams			✓		
6	Ability to link theory to practice				✓	
7	How do you rate the course/curriculum content that you have learnt in relation to your current job				✓	
8	Compatibility with industry standards				✓	

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Suggestions: (1) The curriculum for VLSI concepts need to be broadened.

(2) Syllabus should cover Static - Timing analysis of Digital circuits. Knowledge in this domain is highly valued in Industry.

(3) There should be some chapters on die fabrication & power delivery to chip.

(4) Syllabus should focus more on Short-Channel effects, FIN-FET's & Silicon on Insulator technology.

Swaroop
Signature

Sapthagiri College of Engineering

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ELECTRONICS AND COMMUNICATION ENGINEERING

CIRCULAR

Date: 23/05/2016

This is to inform that there will be a meeting of Academic committee members for analyzing curriculum syllabus of academic year 2016-17. The meeting is scheduled on 24/05/2016 at 10.30 AM in HODs chamber.

Sl No.	Faculty Name	Designation	Signature
1.	Prof.Agalya P.	Associate Professor	
2.	Prof.Shobha S.	Associate Professor	
3.	Prof. Ravishankara M. N.	Associate Professor	
4.	Prof. Shobha I Hugar	Assistant Professor	

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HOD

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ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 24/05/2016

MINUTES OF MEETING

With reference to circular dated on 23/05/2016, the academic committee member assembled in HODs chamber for addressing the following agenda.

Agenda:

- Reviewing the department curriculum syllabus of Academic Year 2016-17
- Reviewing the feedback analysis of various stake holders of the academic year 2015-16
- Identifying the gaps in the syllabus
- Action to be taken for the identified gaps.

During the meeting the following members were present

Sl No.	Faculty Name	Designation	Signature
1.	Prof.Agalya P.	Associate Professor	
2.	Prof.Shobha S.	Associate Professor	
3.	Prof. Ravishankara M. N.	Associate Professor	
4.	Prof. Shobha I Hugar	Assistant Professor	

The following points were discussed in the meeting

1. The committee members reviewed the department curriculum syllabus.
2. The committee members discussed about the feedback analysis of department curriculum syllabus.
3. The members identified the gaps based on the analysis.
4. The following actions were taken for the gaps that are identified.

SL.NO	SEM	Course Title	Identified Gap
1	VI-A/B	Fundamental of CMOS VLSI	Lack of practical implementation concepts

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ELECTRONICS AND COMMUNICATION ENGINEERING

Action Taken:

Based on the feedback obtained from Students, Faculty, Alumni and employer and analysis of syllabus by department academic committee members, it was decided to conduct certification course on VLSI – ASIC Design to overcome the gaps identified in the syllabus.

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ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 27/05/2016

To

IQAC Coordinator

Sapthagiri College of Engineering

Bengaluru-560 057

Respected sir/madam,

Subject: Requisition for conduction of certification course and approval from Governing Council.

With respect to the Academic committee members meeting held for analyzing department curriculum/syllabus for the academic year 2016-17. The committee members identified few gaps after analyzing the syllabus and feedback from the stakeholders. To bridge the gaps identified in the curriculum, the committee members decided to conduct a certification course on VLSI – ASIC Design from 25.07.2016 to 29.07.2016 for the academic year 2016-17. So, I request you to forward and get the approval from the governing council for the same.

Thanking You,

Enclosure: Budget Proposal.

Forwarded for the GC approval for ratification

HOD
Head of the Department
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ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 27-05-2016

To,

THE IQAC Coordinator

Sapthagiri College of Engineering

Bangalore - 560057.

Respected Sir,

Subject: Budget Proposal for conduction of certification program on "VLSI - ASIC Design"

The Budget Proposal for conduction a certification program on" VLSI - ASIC Design" from 25-07-2016 to 29-07-2016 is hereby enclosed for your kind consideration and approval.

The details of the Recurring budget are given as follows:

Recurring Amount:

Sl. No.	Description	Quantity	Amount in Rs.
1	Bouquet	1	200
2	Certificates	No. of Students	1500
3	Others		1000
Total			2700

Forwarded for the GC approval for ratification

HOD

Head of the Department
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ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 12-07-2016

CIRCULAR

This is to inform that the following Academic Committee members are requested to attend the meeting on 13/07/2016 at 10.30AM in the HODs chamber to decide the syllabus and the esson plan for the certification program on "VLSI - ASIC Design"

Sl No.	Faculty Name	Designation	Signature
1.	Prof.Agalya P.	Associate Professor	
2.	Prof.Shobha S.	Associate Professor	
3.	Prof. Ravishankara M. N.	Associate Professor	
4.	Prof. Shobha I Hugar	Associate Professor	

HOD
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ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 12-07-2016

To,

Mr.Venkatesh
Intel Technology India Private limited
Lead Engineer
Bangalore

Respected Sir,

Subject: Invitation as a "Guest Speaker" in certification program and to attend meeting to discuss about the certification program

Department of Electronics & Communication Engineering have planned to conduct a certification program titled "VLSI - ASIC Design"for 7th semester students from 25-07-2016 to 29-07-2016. In this connection, we are privileged to invite you as a guest speaker on the above mentioned topic.

Thanking you for your kind acceptance to our request on phone. We request you to attend the meeting to discuss about the conduction of certification course on 13/07/2016 at 10:30 AM. We look forward to welcome you at SCE.

Thanking you

Yoursfaithfully

HOD

Head of the Department
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ELECTRONICS AND COMMUNICATION ENGINEERING

13-07-2016

Minutes of Meeting

A meeting was conducted on 13-07-2016 in ECE HOD's Chamber to discuss and approve the syllabus & schedule of the 5 days Certification Course for VII semester ECE Students.

- **Course Title :** VLSI - ASIC Design
- **Resource Personnel :** Mr. Venkatesh, Lead Engineer, Intel Technology India Pvt. Ltd. Bangalore & team
- **Course Duration & Date:** 5 Days from 25-07-2016 to 29-07-2016

Syllabus & Schedule of the certification program

Date	Time	Topics	Hours
25.07.2016	8:30 AM - 10:15 AM	Introduction to VLSI Design, Full custom, Semi custom, ASIC and FPGA design.	6.30hrs.
	10:30 AM – 12:30 AM	Fundamentals of Digital IC Design, VLSI Design flow -Overview, Semicustom IC Design – Requirements	
	1:30PM – 3PM	ASIC Design flow, RTL Synthesis of HDL – Synthesis guidelines, Synthesis and Simulation Mismatches	
	3.15PM – 4.30pm	Hands on session on getting started with RTL Complier	
26.07.2016	8:30 AM - 10:15 AM	Gate Level Netlist–Concepts and key terminologies, Functional Simulation and synthesis of the given design	6.30hrs.
	10:30 AM – 12:30 AM	Functional Simulation and synthesis of the given design: Hands on	
	1:30PM – 3PM	RTL Synthesis of a given design block: Hands on	
	3.15PM – 4.30pm	RTL Synthesis of a given design block: Hands on	
27.07.2016	8:30 AM - 10:15 AM	Physical Design flow – Theory Concepts and Tool, Basics of Physical Design – PVT Corners, Inputs for PD, Basics of Chip	6.30hrs.
	10:30 AM – 12:30 AM	Fabrication, Timing, Clock Gating, Interpreting the Design Specifications	

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ELECTRONICS AND COMMUNICATION ENGINEERING

	1:30PM – 3PM	Physical Design flow – Netlist & Floor planning, Placement Analysis of individual blocks of a design: Hands on	
	3.15PM – 4.30pm	Netlist and Floor planning: Hands on	
28.07.2015	8:30 AM - 10:15 AM	Physical Design flow and Physical Verification	6.30hrs.
	10:30 AM – 12:30 AM	Physical Design flow – Clock Tree Synthesis (CTS)	
	1:30PM – 3PM	Physical Design flow – Routing	
	3.15PM – 4.30pm	Routing	
29.07.2015	8:30 AM - 10:15 AM	Physical Verification – Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks	6.30hrs.
	10:30 AM – 12:30 AM	Hands on session: Routing	
	1:30PM – 3PM	Hands on session: Physical Verification	
	3.15PM – 4.30pm	Hands on session: Physical Verification	

The following members were present in the meeting and the syllabus and lesson plan for the certification program has been decided.

Sl. No.	Faculty Name	Designation	Signature
1.	Prof.Agalya P.	Associate Professor	
2.	Prof.Shobha S.	Associate Professor	
3.	Prof. Ravishankara M. N.	Associate Professor	
4.	Prof. Shobha I Hugar	Assistant Professor	
5.	Mr.Venkatesh	Guest Speaker	

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ELECTRONICS AND COMMUNICATION ENGINEERING

18.07.16

NOTICE

As a part of programming skill development Department of Electronics and Communication Engineering is conducting Five days Certification Course on "VLSI - ASIC Design" from 25-07-2016 to 29-07-2016. VII semester students of ECE are informed to attend the course compulsorily.

HOD

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Electronics and Communication Engineering

Academic Year: 2016-17

List of Students enrolled for the certification course on "VLSI – ASIC Design"

Sl. No	USN	Name of the Students	Semester & Sec
1.	1SG12EC122	YOGESH N	VII A
2.	1SG13EC001	A NITHIN KUMAR	VII A
3.	1SG13EC002	AASHISH BIRADAR	VII A
4.	1SG13EC005	ABHISHEK N R	VII A
5.	1SG13EC006	ADARSH S	VII A
6.	1SG13EC007	AISHWARYA R	VII A
7.	1SG13EC008	AKASH PRABHAKAR	VII A
8.	1SG13EC011	ALI ASGAR KHAN	VII A
9.	1SG13EC013	AMAN MAKRANI	VII A
10.	1SG13EC014	AMBIKA R B	VII A
11.	1SG13EC015	ANJALI RAJ	VII A
12.	1SG13EC016	ANKUR ANAND	VII A
13.	1SG13EC017	ANUPAMA M A	VII A
14.	1SG13EC018	ARCHANA PANIGRAHI	VII A
15.	1SG13EC021	ARPITHA H S	VII A
16.	1SG13EC023	BABA FAKRUDDIN R	VII A
17.	1SG13EC024	BENAKA PRASAD S T	VII A
18.	1SG13EC025	BHARATH V	VII A
19.	1SG13EC027	CHITHRA H S	VII A
20.	1SG13EC028	DASHAVANTH K	VII A
21.	1SG13EC030	GAURAV RANJAN	VII A
22.	1SG13EC031	GUNA SHEKAR G	VII A
23.	1SG13EC033	HARSH KOTHARI	VII A
24.	1SG13EC034	HARSHITHA R	VII A
25.	1SG13EC035	JAYANTHI SRI HARIPRIYA	VII A
26.	1SG13EC036	KALPANA K	VII A
27.	1SG13EC037	KARAN BHARTI	VII A
28.	1SG13EC038	KARTHIK H R	VII A
29.	1SG13EC039	KAVANA S THEERTHA	VII A
30.	1SG13EC040	KAVYASHREE K T	VII A
31.	1SG13EC041	KHUSHBU	VII A
32.	1SG13EC042	KOMALA B	VII A
33.	1SG13EC043	KUSHAL GOWDA B	VII A
34.	1SG13EC044	LAVANYA M	VII A
35.	1SG13EC045	M ABHILASH	VII A
36.	1SG13EC049	MAHADEVA N	VII A
37.	1SG13EC050	MANASA J	VII A
38.	1SG13EC053	MANISHA S	VII A
39.	1SG13EC054	MEGHANA H V	VII A
40.	1SG13EC055	MINAKSHI KUMARI	VII A
41.	1SG13EC057	NAGAVENI H	VII A
42.	1SG13EC058	NAMRATHA	VII A

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Electronics and Communication Engineering

43.	1SG13EC059	NANCY M	VII A
44.	1SG13EC061	NEHA KAMATH G	VII A
45.	1SG13EC062	NETHRAVATHI V	VII A
46.	1SG13EC063	NIKHIL NARAYANA K	VII A
47.	1SG13EC064	NISHA K MERTA	VII A
48.	1SG13EC065	NITHIN J	VII A
49.	1SG13EC066	P BOUNESH	VII A
50.	1SG14EC403	CHANDRASHEKAR GOWDA	VII A
51.	1SG14EC404	DIWAKARA	VII A
52.	1SG14EC405	ESHWAR M	VII A
53.	1SG14EC406	GANGARAM B P	VII A
54.	1SG14EC407	HARINI C	VII A
55.	1SG14EC408	HARSHITHA B N	VII A
56.	1SG13EC127	GOWTHAM N	VII A
57.	1SG13EC128	ANUP KUMAR	VII A
58.	1SG13EC129	RAJU B L	VII A
59.	1SG13EC130	NIKKHILESH	VII A
60.	1SG09EC071	SUNITH VEERESH	VII B
61.	1SG10EC080	SHRUTHI B J	VII B
62.	1SG11EC007	AMRIT RAJ	VII B
63.	1SG11EC019	CHANDRASHEKARA N	VII B
64.	1SG11EC049	PAVAN P(YB)	VII B
65.	1SG11EC079	SOURABH KUMAR SINGH	VII B
66.	1SG12EC411	MURUGESH P D	VII B
67.	1SG13EC401	AKSHATHA V P	VII B
68.	1SG13EC407	CHAITHRA G C	VII B
69.	1SG13EC418	RAFI J	VII B
70.	1SG12EC072	PRAJWALA S	VII B
71.	1SG12EC120	VIVEK KUMAR SINGH	VII B
72.	1SG13EC067	P PRAJWAL	VII B
73.	1SG13EC070	PRASHANT KUMAR RAJPUT	VII B
74.	1SG13EC071	PRAVESH P JAIN	VII B
75.	1SG13EC073	PRIYA B U	VII B
76.	1SG13EC074	PRIYA K R	VII B
77.	1SG13EC076	PRIYA V	VII B
78.	1SG13EC077	PRIYANKA G	VII B
79.	1SG13EC078	PRIYANKA M	VII B
80.	1SG13EC079	PRIYANKA N H	VII B
81.	1SG13EC080	PRUTHVI U	VII B
82.	1SG13EC081	RAHUL	VII B
83.	1SG13EC082	RAHUL KUMAR V	VII B
84.	1SG13EC084	RAKESH BHAT K H	VII B
85.	1SG13EC085	RAKESH J	VII B
86.	1SG13EC086	RAKESH M PEEDI	VII B
87.	1SG13EC092	ROOPAISHWARYA T B	VII B
88.	1SG13EC093	S SHARAN	VII B
89.	1SG13EC094	SAHANA N	VII B

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#14/5, Chikkasandra, Hesaraghatta Main Road, Bengaluru – 560057

Electronics and Communication Engineering

90.	1SG13EC096	SANJAY M E	VII B
91.	1SG13EC097	SAROJ KUMAR SINGH	VII B
92.	1SG13EC099	SHARIQUE ANWAR	VII B
93.	1SG13EC101	SHOBHA R	VII B
94.	1SG13EC102	SHRAVAN ASHOK	VII B
95.	1SG13EC104	SHRUTHI B	VII B
96.	1SG13EC106	SHYAM SEBASTIN	VII B
97.	1SG13EC108	SONIA YADAV	VII B
98.	1SG13EC109	SPOORTHI Y	VII B
99.	1SG13EC110	SRIMOYE SANJOY PAL	VII B
100.	1SG13EC111	SUKHPREET KAUR	VII B
101.	1SG13EC112	SUNIL KUMAR PATIL	VII B
102.	1SG13EC113	SUPRITH M	VII B
103.	1SG13EC114	SUSHMA N	VII B
104.	1SG13EC115	SUSHMITHA R	VII B
105.	1SG13EC117	V MEGHANA MENON	VII B
106.	1SG13EC118	VARALAKSHMI H C	VII B
107.	1SG13EC119	VEENA R	VII B
108.	1SG13EC120	VENKATESH G	VII B
109.	1SG13EC121	VIKAS MUDGAL	VII B
110.	1SG13EC123	VISHWAJITH V BHARADWAJ	VII B
111.	1SG13EC125	YASHWANTH K HEGDE	VII B
112.	1SG13EC126	YOGESH N	VII B
113.	1SG14EC410	PREETHI	VII B
114.	1SG14EC411	PREMANJALI V	VII B
115.	1SG14EC415	RAVI K	VII B
116.	1SG14EC416	SACHIN S	VII B
117.	1SG14EC417	SOUJANYA G A	VII B
118.	1SG14EC418	SRINIVAS T	VII B
119.	1SG14EC420	SWATHI CHOUGALA	VII B

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Coordinator

HOD

Head of the Department
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Sapthagiri College of Engineering
Bangalore 560 057

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Electronics and Communication Engineering

Academic Year: 2016-17

List of Students enrolled for the certification course on "VLSI – ASIC Design"

Sl. No	USN	Name of the Students	25.07.2016		26.07.2016		27.07.2016		28.07.2016		29.07.2016	
			MS	AS	MS	AS	MS	AS	MS	AS	MS	AS
1.	1SG12EC122	YOGESH N	1	2	3	3	4	5	6	7	8	8
2.	1SG13EC001	A NITHIN KUMAR	1	2	3	4	5	6	7	8	9	10
3.	1SG13EC002	AASHISH BIRADAR	1	2	3	4	4	5	6	6	7	8
4.	1SG13EC005	ABHISHEK N R	1	2	3	3	4	5	5	6	7	8
5.	1SG13EC006	ADARSH S	1	2	3	3	4	5	6	7	8	9
6.	1SG13EC007	AISHWARYA R	1	2	3	4	5	6	7	8	9	10
7.	1SG13EC008	AKASH PRABHAKAR	1	2	3	4	5	6	7	8	9	10
8.	1SG13EC011	ALI ASGAR KHAN	1	2	3	3	4	5	6	6	7	8
9.	1SG13EC013	AMAN MAKRANI	1	2	3	4	5	6	7	8	9	10
10.	1SG13EC014	AMBIKA R B	1	2	3	4	5	6	7	8	9	10
11.	1SG13EC015	ANJALI RAJ	1	2	3	3	4	5	6	7	8	9
12.	1SG13EC016	ANKUR ANAND	1	2	3	4	5	5	6	7	8	9
13.	1SG13EC017	ANUPAMA M A	1	2	3	3	4	5	6	7	8	8
14.	1SG13EC018	ARCHANA PANIGRAHI	1	2	3	4	5	6	6	7	8	9
15.	1SG13EC021	ARPITHA H S	1	2	3	4	5	5	6	6	7	8
16.	1SG13EC023	BABA FAKRUDDIN R	1	2	2	3	4	5	6	7	8	9
17.	1SG13EC024	BENAKA PRASAD S T	1	2	3	4	5	6	7	8	9	10
18.	1SG13EC025	BHARATH V	1	2	3	4	5	5	6	7	7	8
19.	1SG13EC027	CHITHRA H S	1	2	3	4	5	6	7	8	9	10
20.	1SG13EC028	DASHAVANTH K	1	2	2	3	4	5	6	7	8	9
21.	1SG13EC030	GAURAV RANJAN	1	2	3	4	5	6	7	8	9	10
22.	1SG13EC031	GUNA SHEKAR G	1	2	3	4	5	6	7	8	9	10
23.	1SG13EC033	HARSH KOTHARI	1	2	2	3	4	4	5	6	7	8
24.	1SG13EC034	HARSHITHA R	1	2	3	4	5	6	7	8	9	10
25.	1SG13EC035	JAYANTHI SRI HARIPRIYA	1	2	3	4	5	6	7	8	9	10
26.	1SG13EC036	KALPANA K	1	2	3	4	4	5	5	6	7	8
27.	1SG13EC037	KARAN BHARTI	1	2	3	4	5	6	7	8	9	10
28.	1SG13EC038	KARTHIK H R	1	2	3	3	4	5	6	7	8	9
29.	1SG13EC039	KAVANA S THEERTHA	1	2	3	4	4	5	5	6	7	8
30.	1SG13EC040	KAVYASHREE K T	1	2	3	4	5	6	7	8	9	10
31.	1SG13EC041	KHUSHBU	1	2	3	3	4	5	6	7	8	9
32.	1SG13EC042	KOMALA B	1	2	3	4	5	6	7	8	8	9
33.	1SG13EC043	KUSHAL GOWDA B	1	2	3	4	5	5	6	6	7	8
34.	1SG13EC044	LAVANYA M	1	2	2	3	4	5	5	6	7	8
35.	1SG13EC045	M ABHILASH	1	2	3	3	4	5	6	7	8	9
36.	1SG13EC049	MAHADEVA N	1	2	2	3	4	5	6	7	8	9
37.	1SG13EC050	MANASA J	1	2	3	4	5	6	7	8	9	9
38.	1SG13EC053	MANISHA S	1	1	2	3	4	5	6	7	8	9

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39.	1SG13EC054	MEGHANA H V	1	2	3	4	5	5	6	7	7	8
40.	1SG13EC055	MINAKSHI KUMARI	1	2	3	4	5	6	7	8	9	10
41.	1SG13EC057	NAGAVENI H	1	2	2	3	4	5	6	7	8	9
42.	1SG13EC058	NAMRATHA	1	2	2	3	4	5	5	7	8	9
43.	1SG13EC059	NANCY M	1	1	2	3	3	4	5	6	7	8
44.	1SG13EC061	NEHA KAMATH G	1	2	3	4	5	6	7	8	8	9
45.	1SG13EC062	NETHRAVATHI V	1	2	3	4	4	5	5	6	7	8
46.	1SG13EC063	NIKHIL NARAYANA K	1	2	2	3	4	5	6	7	8	9
47.	1SG13EC064	NISHA K MERTA	1	2	3	4	5	6	7	8	9	9
48.	1SG13EC065	NITHIN J	1	2	3	4	4	5	5	6	7	8
49.	1SG13EC066	P BOUNESH	1	2	2	3	4	5	6	7	8	9
50.	1SG14EC4[illegible]	CHANDRASHEKAR GOWDA	1	2	3	4	5	6	7	8	9	9
51.	1SG14EC404	DIWAKARA	1	2	3	4	5	5	6	7	8	9
52.	1SG14EC405	ESHWAR M	1	2	3	4	5	5	6	7	8	9
53.	1SG14EC406	GANGARAM B P	1	2	3	4	5	5	6	7	8	9
54.	1SG14EC407	HARINI C	1	2	2	3	4	5	6	7	8	8
55.	1SG14EC408	HARSHITHA B N	1	2	3	3	4	5	6	7	8	9
56.	1SG13EC127	GOWTHAM N	1	2	2	3	4	5	6	7	8	9
57.	1SG13EC128	ANUP KUMAR	1	2	2	3	4	5	6	7	8	9	10
58.	1SG13EC129	RAJU B L	1	1	2	3	4	5	6	7	8	9	10
59.	1SG13EC131	NIKKHILESH	1	1	2	3	4	5	6	7	7	8
60.	1SG09EC071	SUNITH VEERESH	1	2	3	4	5	5	5	6	7	8
61.	1SG10EC080	SHRUTHI B J	1	2	3	4	5	6	7	8	9	10
62.	1SG11EC007	AMRIT RAJ	1	2	3	4	5	6	7	8	9	10
63.	1SG11EC019	CHANDRASHEKAR A N	1	2	3	4	5	5	6	7	8	9
64.	1SG11EC049	PAVAN P(YB)	1	2	3	3	4	5	6	7	8	9
65.	1SG11EC075	SOURABH KUMAR SINGH	1	2	3	4	5	6	7	8	9	10
66.	1SG12EC411	MURUGESH P D	1	1	2	3	4	5	6	7	8	9
67.	1SG13EC401	AKSHATHA V P	1	1	2	3	4	5	6	7	8	9
68.	1SG13EC407	CHAITHRA G C	1	1	2	2	3	4	5	6	7	8
69.	1SG13EC418	RAFI J	1	2	3	4	5	6	7	8	9	10
70.	1SG12EC072	PRAJWALA S	1	2	3	4	5	6	6	7	8	9
71.	1SG12EC120	VIVEK KUMAR SINGH	1	2	3	4	5	6	6	7	8	9
72.	1SG13EC067	P PRAJWAL	1	1	2	3	4	5	6	7	8	9
73.	1SG13EC070	PRASHANT KUMAR RAJPUT	1	2	3	3	4	5	6	7	8	9
74.	1SG13EC071	PRAVESH P JAIN	1	2	3	4	4	5	6	6	7	8
75.	1SG13EC073	PRIYA B U	1	2	3	4	5	6	7	8	8	9
76.	1SG13EC074	PRIYA K R	1	2	3	3	4	5	6	7	8	9
77.	1SG13EC076	PRIYA V	1	2	3	4	5	5	6	7	8	9
78.	1SG13EC077	PRIYANKA G	1	2	3	4	4	5	5	6	7	8
79.	1SG13EC078	PRIYANKA M	1	2	3	4	4	5	6	7	8	9
80.	1SG13EC079	PRIYANKA N H	1	2	3	4	5	6	7	8	9	10
81.	1SG13EC080	PRUTHVI U	1	2	3	4	5	6	7	8	9	10
82.	1SG13EC081	RAHUL	1	2	3	4	5	5	6	7	8	8
				2	3	4	5	5	6	7	8	9

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83.	1SG13EC082	RAHUL KUMAR V	1	2	3	4	5	6	7	8	8	9
84.	1SG13EC084	RAKESH BHAT K H	1	2	3	3	4	5	6	7	8	8
85.	1SG13EC085	RAKESH J	1	2	3	4	5	6	7	8	9	10
86.	1SG13EC086	RAKESH M PEEDI	1	2	2	3	4	5	6	7	8	9
87.	1SG13EC092	ROOPAISHWARYA T B	1	2	3	3	4	5	6	7	8	9
88.	1SG13EC093	S SHARAN	1	2	2	3	4	5	6	6	7	8
89.	1SG13EC094	SAHANA N	1	2	3	4	5	6	7	8	9	10
90.	1SG13EC096	SANJAY M E	1	2	3	4	5	6	7	8	9	10
91.	1SG13EC097	SAROJ KUMAR SINGH	1	2	3	4	5	6	6	7	8	9
92.	1SG13EC099	SHARIQUE ANWAR	1	2	2	3	4	5	5	6	7	8
93.	1SG13EC101	SHOBHA R	1	2	3	4	5	5	5	7	8	8
94.	1SG13EC102	SHRAVAN ASHOK	1	2	3	4	5	6	7	8	9	10
95.	1SG13EC104	SHRUTHI B	1	2	3	3	4	5	6	7	8	8
96.	1SG13EC106	SHYAM SEBASTIN	1	2	2	3	4	5	6	7	8	9
97.	1SG13EC108	SONIA YADAV	1	2	3	4	5	6	7	8	9	10
98.	1SG13EC109	SPOORTHI Y	1	2	3	4	5	5	6	7	8	9
99.	1SG13EC110	SRIMOYE SANJOY PAL	1	2	3	4	5	6	7	8	9	10
100.	1SG13EC111	SUKHPREET KAUR	1	2	3	4	4	5	6	6	7	8
101.	1SG13EC112	SUNIL KUMAR PATIL	1	1	2	3	4	5	6	7	8	9
102.	1SG13EC113	SUPRITH M	1	2	3	4	5	6	7	8	9	10
103.	1SG13EC114	SUSHMA N	1	2	3	4	5	6	7	8	9	10
104.	1SG13EC115	SUSHMITHA R	1	1	2	3	4	5	6	7	8	9
105.	1SG13EC117	V MEGHANA MENON	1	2	3	4	5	5	6	7	8	9
106.	1SG13EC118	VARALAKSHMI H C	1	2	3	3	4	5	6	7	8	9
107.	1SG13EC119	VEENA R	1	2	3	4	5	5	6	7	8	9
108.	1SG13EC120	VENKATESH G	1	1	2	3	4	4	5	6	7	8
109.	1SG13EC121	VIKAS MUDGAL	1	2	3	3	4	5	6	7	8	9
110.	1SG13EC123	VISHWAJITH V BHARADWAJ	1	2	3	4	5	6	7	7	8	9
111.	1SG13EC125	YASHWANTH K HEGDE	1	2	3	4	5	5	6	7	8	9
112.	1SG13EC126	YOGESH N	1	2	3	3	4	5	6	7	8	9
113.	1SG14EC410	PREETHI	1	1	2	3	4	5	5	6	7	8
114.	1SG14EC411	PREMANJALI V	1	2	3	4	5	6	7	8	9	10
115.	1SG14EC415	RAVI K	1	2	2	3	4	5	6	7	8	9
116.	1SG14EC416	SACHIN S	1	2	3	4	5	6	7	8	9	10
117.	1SG14EC417	SOUJANYA G A	1	2	3	4	5	6	7	8	9	10
118.	1SG14EC418	SRINIVAS T	1	1	2	3	4	5	6	7	8	9
119.	1SG14EC420	SWATHI CHOUGALA	1	2	3	4	5	6	7	8	9	10

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ELECTRONICS AND COMMUNICATION ENGINEERING

5 days Certification Course on "VLSI - ASIC Design"

Test Time Table

Sl. No.	DATE	DAY	TIMINGS
1	05-08-2016	Friday	3.00PM-4.00PM

HOD
Head of the Department
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Bangalore 560 057

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ELECTRONICS AND COMMUNICATION ENGINEERING

5 days Certification Course " VLSI - ASIC Design

Question Paper

Date : 05.08.2016

Duration :1hr

Maximum marks :50

Note: Question number 1-20 (1Mark each)

Question No. 21 (30 Marks)

Answer all the Questions:

1) The utilization of CAD tools for drawing timing waveform diagram and transforming it into a network of logic gates is known as _____.

a. Waveform Editor

b. Waveform Estimator

c. Waveform Simulator

d. Waveform Evaluator

2) Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?

a. Simulation

b. Optimization

c. Synthesis

d. Verification

3) _____ is the fundamental architecture block or element of a target PLD.

a. System Partitioning

b. Pre-layout Simulation

c. Logic cell

d. Post-layout Simulation

4) In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?

a. Floor planning

b. Placement & Routing

c. Testing

d. Extraction

5) Among the VHDL features, which language statements are executed at the same time in parallel flow?

a. Concurrent

b. Sequential

c. Net-list

d. Test-bench

6) In Net-list language, the net-list is generated _____synthesizing VHDL code.

a. Before

b. At the time of (during)

c. After

d. None of the above

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7) In VHDL, which object/s is/are used to connect entities together for the model formation?
a. Constant
b. Variable
c. Signal
d. All of the above

8) Which data type in VHDL is non synthesizable & allows the designer to model the objects of dynamic nature?
a. Scalar
b. Access
c. Composite
d. File

9) Which type of simulation mode is used to check the timing performance of a design?
a. Behavioural
b. Switch-level
c. Transistor-level
d. Gate-level

10) In the simulation process, which step specifies the conversion of VHDL intermediate code so that it can be used by the simulator?
a. Compilation
b. Elaboration
c. Initialization
d. Execution

11) Which type of simulator/s neglect/s the intra-cycle state transitions by checking the status of target signals periodically irrespective of any events?
a. Event-driven Simulator
b. Cycle-based Simulator
c. Both a and b
d. None of the above

12) Which among the following is not a characteristic of 'Event-driven Simulator'?
a. Identification of timing violations
b. Storage of state values & time information
c. Time delay calculation
d. No event scheduling

13) Which among the following is an output generated by synthesis process?
a. Attributes & Library
b. RTL VHDL description
c. Circuit constraints
d. Gate-level net list

14) Register transfer level description specifies all of the registers in a design & _____ logic between them.
a. Sequential
b. Combinational
c. Both a and b

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d. None of the above

15) In synthesis process, the load attribute specify/ies the existing amount of _____load on a particular output signal.

a. Inductive

b. Resistive

c. Capacitive

d. All of the abov

16) Which attribute in synthesis process specify/ies the resistance by controlling the quantity of current it can source?

a. Load attribute

b. Drive attribute

c. Arrival time attribute

d. All of the above

17) Which type of digital systems exhibit the necessity for the existence of at least one feedback path from output to input?

a. Combinational System

b. Sequential system

c. Both a and b

d. None of the above

18) The output of sequential circuit is regarded as a function of time sequence of _____.

A. Inputs

B. Outputs

C. Internal States

D. External States

a. A & D

b. A & C

c. B & D

d. B & C

19) The time required for an input data to settle _____ the triggering edge of clock is known as 'Setup Time'.

a. Before

b. During

c. After

d. All of the above

20) Hold time is defined as the time required for the data to _____ after the triggering edge of clock.

a. Increase

b. Decrease

c. Remain stable

d. All of the above

21) Design a logical circuit Y=AB+CD and do the physical verification.

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ELECTRONICS AND COMMUNICATION ENGINEERING

Approved by Academic Committee Members & Guest Speaker

Sl No.	Faculty Name	Designation	Signature
1.	Prof.Agalya P.	Associate Professor	
2.	Prof.Shobha S.	Associate Professor	
3.	Prof. Ravishankara M. N.	Associate Professor	
4.	Prof. Shobha I Hugar	Associate Professor	
5.	Mr.Venkatesh	Guest Speaker	

Head of the Department
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ELECTRONICS AND COMMUNICATION ENGINEERING

5 days Certification Course on "VLSI - ASIC Design Solutions

Duration :1hr **Maximum marks :**50

Note: Question number 1-20 (1M each)
Question number 21 (20M)

Answer all the Questions

1) The utilization of CAD tools for drawing timing waveform diagram and transforming it into a network of logic gates is known as _____.

a. Waveform Editor
b. Waveform Estimator
c. Waveform Simulator
d. Waveform Evaluator

ANSWER: Waveform Editor

2) Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?

a. Simulation
b. Optimization
c. Synthesis
d. Verification

ANSWER: Synthesis

3) _____ is the fundamental architecture block or element of a target PLD.

a. System Partitioning
b. Pre-layout Simulation
c. Logic cell
d. Post-layout Simulation

ANSWER: Logic cell

4) In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?

a. Floorplanning
b. Placement & Routing
c. Testing
d. Extraction

ANSWER: Extraction

5) Among the VHDL features, which language statements are executed at the same time in parallel flow?

a. Concurrent
b. Sequential
c. Net-list
d. Test-bench

ANSWER: Concurrent

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6) In Net-list language, the net-list is generated _____synthesizing VHDL code.
a. Before
b. At the time of (during)
c. After
d. None of the above
ANSWER: After

7) In VHDL, which object/s is/are used to connect entities together for the model formation?
a. Constant
b. Variable
c. Signal
d. All of the above
ANSWER: Signal

8) Which data type in VHDL is non synthesizable & allows the designer to model the objects of dynamic nature?
a. Scalar
b. Access
c. Composite
d. File
ANSWER: Access

9) Which type of simulation mode is used to check the timing performance of a design?
a. Behavioural
b. Switch-level
c. Transistor-level
d. Gate-level
ANSWER: Gate-level

10) In the simulation process, which step specifies the conversion of VHDL intermediate code so that it can be used by the simulator?
a. Compilation
b. Elaboration
c. Initialization
d. Execution
ANSWER: Elaboration

11) Which type of simulator/s neglect/s the intra-cycle state transitions by checking the status of target signals periodically irrespective of any events?
a. Event-driven Simulator
b. Cycle-based Simulator
c. Both a and b
d. None of the above
ANSWER: Cycle-based Simulator

12) Which among the following is not a characteristic of 'Event-driven Simulator'?
a. Identification of timing violations
b. Storage of state values & time information
c. Time delay calculation

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c No event scheduling

ANSWER: No event scheduling

13) Which among the following is an output generated by synthesis process?

a. Attributes & Library

b. RTL VHDL description

c. Circuit constraints

d Gate-level net list

ANSWER: Gate-level net list

14) Register transfer level description specifies all of the registers in a design & _____ logic between them.

a. Sequential

b. Combinational

c. Both a and b

d. None of the above

ANSWER: Combinational

15) In synthesis process, the load attribute specify/ies the existing amount of _____load on a particular output signal.

a. Inductive

b. Resistive

c. Capacitive

d. All of the abov

16) Which attribute in synthesis process specifies the resistance by controlling the quantity of current it can source?

a. Load attribute

b. Drive attribute

c. Arrival time attribute

d. All of the above

ANSWER: Drive attribute

17) Which type of digital systems exhibit the necessity for the existence of at least one feedback path from output to input?

a. Combinational System

b. Sequential system

c. Both a and b

d. None of the above

ANSWER: Sequential system

18) The output of sequential circuit is regarded as a function of time sequence of _____

A. Inputs

B. Outputs

C. Internal States

D. External States

a. A & D

b. A & C

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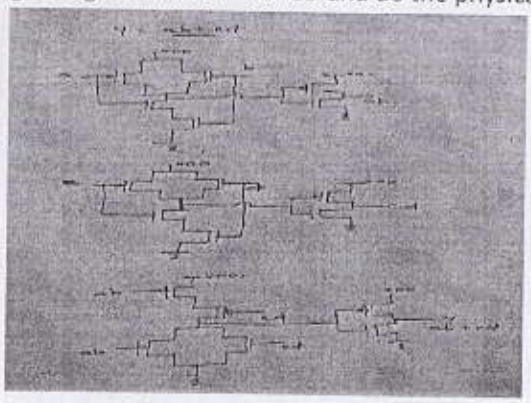
c. B & D
d. B & C
ANSWER: A & C

19) The time required for an input data to settle _____ the triggering edge of clock is known as 'Setup Time'.
a. Before
b. During
c. After
d. All of the above
ANSWER: Before

20) Hold time is defined as the time required for the data to _____ after the triggering edge of clock.
a. Increase
b. Decrease
c. Remain stable
d. All of the above
ANSWER: Remain stable

21) Design a logical circuit Y=AB+CD and do the physical verification.



Approved by Academic Committee Members & Guest Speaker

Sl No.	Faculty Name	Designation	Signature
1.	Prof.Agalya P.	Associate Professor	
2.	Prof.Shobha S.	Associate Professor	
3.	Prof. Ravishankara M. N.	Associate Professor	
4.	Prof. Shobha I Hugar	Associate Professor	
5.	Mr.Venkatesh	Guest Speaker	

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ELECTRONICS AND COMMUNICATION ENGINEERING

5 days Certification Course on "VLSI - ASIC Design"

Participant Feedback

1. How was the overall organization of the Certification Course ?

   a) Poor b) Satisfactory c) Good d) Excellent

2. How appropriate were the facilities provided ?

   a) Poor b) Satisfactory c) Good d) Excellent

3. Opportunity to ask questions for clarification and interaction with presenters

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4. Effectiveness of the Hands-on Sessions

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5. Topic and contents of the Certification Course

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6. How do you rate the Certification Course compared to other workshops that you have attended ?

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7. Generally how was your overall experience during the Certification Course

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8. Any Suggestions:

Nancy. M
Student Name

Student Signature

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8. Any Suggestions:

Preeti
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8. Any Suggestions:

Amrit Raj
Student Name

Student Signature

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8. Any Suggestions:

Priyanka G
Student Name

Student Signature

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8. Any Suggestions:

Spoorthy V

Student Name

Student Signature

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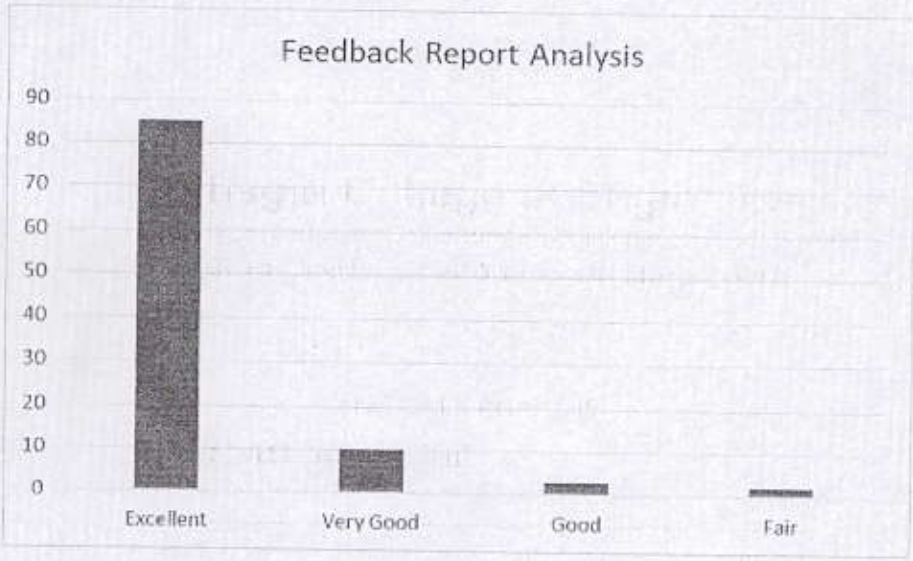
FEEDBACK ANALYSIS

Certification Programme: "VLSI - ASIC Design"

No. of students	Student Feedback (in %)			
	Excellent	Very Good	Good	Fair
45	85	10	3	2



Feedback Report:

85 % of students were completely happy with the certification program and 10 % of students felt it was a good program and remaining 5 % students were satisfied with the program.

Action Taken:

The Feedback report which was collected from the students were sent to the principal and he would take necessary actions based on the comments and conduct more programs for the benefit of students.

CO-ORDINATOR

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ELECTRONICS AND COMMUNICATION ENGINEERING

Certification Course - VLSI - ASIC Design

Post Event Report

Department of ECE conducted Certificate Course on VLSI - ASIC Design and its applications from 25-07-2016 to 29-07-2016.

- **Resource Person** : Mr.Venkatesh, & Team, Intel Technology India Pvt. Ltd. Bengaluru
- **Duration of the course** :Five days from 25 - 07 -2016 to 29 - 07- 2016.

Objective of the Course: The five day course made the students to be familiar with the major concepts in VLSI - ASIC Design which is a main platform for their career .Certificate Course became the vital step to improve the knowledge of students

Session wise Report

Date	Report
25.07.2016	Speaker delivered talk on Introduction to VLSI Design, Full custom, Semi custom, ASIC and FPGA design, its Significance and compiler
26.07.2016	Speaker delivered talk and Hands on session on RTL Synthesis and Functional Simulation
27.07.2016	Speaker delivered talk on Physical Design flow – Theory Concepts and Tool, Basics of Physical Design
28.07.2016	Speaker delivered talk and Hands on session on Physical Design flow
29.07.2016	Speaker delivered talk and Hands on session on Physical Verification – Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks, Routing an floor planning

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Students with Resource Person in ASIC Design Certification course

Conclusion:

The optimistic learning environment prompted motivation in the learning of the students. They felt bonhomie after the course they took. A sense of satisfaction was also seen. Faculty members were also equally benefited with the course. They felt more expedient while delivering the lectures as the margin was erased between these students and others. A structured environment was created. This helped in the smooth flow of academic lesson plan by adhering to the timelines. This Course helped the student to improve their knowledge in VLSI - ASIC Design.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Five days certification course on

"VLSI—ASIC DESIGN"

CERTIFICATE

This is to certify that Mr/Ms .....has attended five days certification course on "VLSI—ASIC DESIGN" organized by the Department of Electronics and Communication Engineering, Sapthagiri college of Engineering, Bengaluru from 25th July to 29th July 2016.

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S.C.E., Bengaluru

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CERTIFICATE

This is to certify that Mr/Ms .....AMBIKA R.B.....has attended five days certification course on "VLSI—ASIC DESIGN" organized by the Department of Electronics and Communication Engineering, Sapthagiri college of Engineering, Bengaluru from 25th July to 29th July 2016.

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This is to certify that Mr/Ms .....ANUPAMA . M . A.....has attended five days certification course on "VLSI—ASIC DESIGN" organized by the Department of Electronics and Communication Engineering, Sapthagiri college of Engineering, Bengaluru from 25th July to 29th July 2016.

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CERTIFICATE

This is to certify that Mr/Ms .....ABHISHEK N.R.....has attended five days certification course on "VLSI—ASIC DESIGN" organized by the Department of Electronics and Communication Engineering, Sapthagiri college of Engineering, Bengaluru from 25th July to 29th July 2016.

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