F-QAD-03/R0

SAPTHAGIRI College of Engineering Creating Tomorrow

SAPTHAGIRI COLLEGE OF ENGINEERING,BENGALURU
DEPARTMENT OF MECHANICAL ENGINEERING

COURSE FILE

List of documents

1	Vision and Mission of the Institute
2	Vision and Mission of the Department
3	Subject Allotment Letter
4	Copies of Syllabus-List of text books, reference books, Course Objectives and outcomes
5	Lecture Notes
6	University question papers
7	Calendar of events
8	Personal Time Table & Class Time Table
9	Lesson Plan & Teaching Dairy
10	Student list and Batch list(for lab)
11	Attendance Register
12	Assignment bank/questions
13	Test question papers with Scheme & Solution
14	Test Absentee list- B Form
15	I A Marks: T_1, T_2, T_3, T_{avg} ,Assignment and Final IA
16	Feedback/Assessment by students
17	IA Marks sent to VTU
18	VTU Exam result analysis

Sapthagiri College of Engineering
Department of Electronics and Communication Engineering
VISION & MISSION of the Institution

VISION

The vision of the institution is to create and maintain an enabling learning environment for the students to transform them as thorough professionals to meet diverse professional demands of global environments.

MISSION

The mission of the institution is to provide quality education to the students to pursue courses in different engineering disciplines and to transform their professional dreams into reality and to offer competent budding professionals to the society.

VISION & MISSION of the department

VISION

To be nationally recognized leading educational institute in the field of electronics & communication engineering & an asset to the nation by providing professional engineers to serve the society.

MISSION

To prepare graduates in the field of electronics & communication engineering for prominent careers by providing a broad based knowledge of the fundamentals of engineering & to develop skills that will enable students to contribute effectively in their chosen profession.

Principal
Sapthagiri College of Engineering
Chikkasandra, Hesaraghatta Road,
Bangalore- 560 057

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SAPTHAGIRI COLLEGE OF ENGINEERING

#14/5, Chikkasandra, Hesaraghatta Main Road, Bengaluru- 560 057

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Subject Allotment

(For the Academic Year 2018-19 Even Semester)

Name of the Faculty: **Prof. Agalya P**

Designation: Associate Professor

Sl.No.	Subject	Subject Code	Sem /Sec	Batch
1	ARM Microcontroller & Embedded Systems	15EC62	6 A	-
2	ARM Microcontroller & Embedded Systems	15EC62	6 B	-
3	Embedded Controller Lab	15ECL67	6 A	A1
4	Embedded Controller Lab	15ECL67	6 B	B3

Signature of Faculty

Head of the Department

17/12/18

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SAPTHAGIRI COLLEGE OF ENGINEERING
ACADEMIC YEAR: EVEN 2018-19
(Faculty)

Course	ARM Microcontroller and Embedded System				Course code		15EC62
Faculty	P. Agalya				Semester/Sec		6/A
Core/Elective	Contact Hours /week			Total Hours	Assessment		Credits
Core	L	T	P	50	CIE	SEE	4
	4	-	-		20	80	
Prerequisites	1. Number System 2. Digital Electronics, Digital Integrated circuits 3. Microprocessor, Microcontroller Fundamentals						

Course Objectives

1	Understand the architectural features and instruction set of 32 bit microcontroller ARM Cortex M3.
2	Program ARM Cortex M3 using assembly level instructions and C language for different applications.
3	Understand the basic hardware components of an embedded system and their selection method based on the characteristics and quality attributes.
4	Develop the hardware software co-design and firmware design approaches.
5	Explain the need of real time operating system for embedded system applications.

Syllabus	
MODULE 1	**RBT Level**
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence. (Text 1: Ch 1, 2, 3)	**L1, L2**
MODULE 2	
ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, useful instructions, Assembly and C language Programming. (Text 1: Ch-4, Ch-5, Ch-10 (10.1, 10.2, 10.3, 10.5 only)).	**L1, L2**
MODULE 3	
Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Core of an Embedded System including all types of processor/controller, Memory, Sensors, Actuators, LED, 7 segment LED display, Optocoupler, relay, Piezo buzzer, Push button switch, Communication Interface	**L1,L2, L3**

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(onboard and external types), Embedded firmware, Other system components. (Text 2: All the Topics from Ch-2 & 3, excluding 2.3 & 3.4 (stepper motor), 2.3 & 3.8 (keyboard) and 2.3 & 3.9 (PPI) sections).	
MODULE 4	
Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling (excluding UML), Embedded firmware design and development (excluding C language). (Text 2: Ch-3, Ch-4, Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)	**L1, L2, L3**
MODULE 5	
RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques (Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch 12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)	**L1,L2,L3**

Text Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009.

Course outcomes

At the end of this course the students will be able

CO1	To describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
CO2	To describe the memory map of cortex m3 and apply the knowledge gained for Programming ARM Cortex M3 for different applications.
CO3	To apply the knowledge in selecting basic hardware components in the design of embedded system based on the characteristics and attributes of an embedded system.
CO4	To describe the development of an embedded system using the hardware /software co-design and firmware design approaches.
CO5	To explain the need of real time operating system for embedded system applications.

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CBCS SCHEME

USN | | | | | | | | | | |

15EC62

Sixth Semester B.E. Degree Examination, June/July 2019
ARM Micro Controller and Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the architecture of ARM cortex – M3 processor with neat diagram. **(08 Marks)**
b. With neat diagram, explain operation mode and privilege levels in cortex M3. **(08 Marks)**

OR

2 a. What is stack? Explain push and pop operation. With the help of a neat diagram. **(07 Marks)**
b. Explain in detail special registers used in ARM cortex M3 processor. **(09 Marks)**

Module-2

3 a. Write an ALP to calculate the sum of 1 to 10 numbers. **(08 Marks)**
b. Explain the following instruction set : i) BFC ii) SBFX iii)ASR iv) MRS. **(04 Marks)**
c. Explain how CMSIS provides standard access. Interface for Embedded software. **(04 Marks)**

OR

4 a. Write a program to blink a LED using 'C' language. **(08 Marks)**
b. Explain the following assembler directives AREA, ENTRY, DCB, ALIGN. **(04 Marks)**
c. Explain different bus interfaces supported by cortex M3. **(04 Marks)**

Module-3

5 a. Explain how embedded system are classified. **(08 marks)**
b. With neat block diagram, explain the element of embedded system. **(08 Marks)**

OR

6 a. Differentiate between RISC and CISC. **(04 Marks)**
b. Explain how program memory are classified. **(08 Marks)**
c. Explain how brown-out protection circuits works. **(04 Marks)**

Module-4

7 a. What are the operational and nonoperational attributes of an embedded systems. **(10 Marks)**
b. Explain different types of serial interface bus used in automotive communication. **(06 Marks)**

OR

8 a. Explain fundamental issues in hardware software co-design. **(06 Marks)**
b. Explain with a neat block diagram how source file to object file translation take place. **(06 marks)**
c. Explain super loop based approach of embedded firmware design. **(04 Marks)**

Module-5

9 a. With neat diagram explain operating system architecture. **(08 marks)**

b. Explain how operating systems are classified. **(04 marks)**

c. Differentiate between hard real time system and soft real time system with an example for each. **(04 Marks)**

OR

10 a. With neat diagram, explain embedded system development environment. **(08 marks)**

b. For the following jobs calculate the turnaround time, waiting time using preemptive SJF scheduling algorithm. **(04 Marks)**

Jobs	CPU bust time	Arrival time
1	10	0.0
2	2	3.0
3	1	4.0
4	4	5.0

c. Write a note on IAP [In Application Programming] and in system programming. **(04 Marks)**

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CBCS SCHEME

USN | 1 5 E 1 6 E C 1 2 5 | 15EC62

Sixth Semester B.E. Degree Examination, June/July 2019
ARM Micro Controller and Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the architecture of ARM cortex – M3 processor with neat diagram. **(08 Marks)**
b. With neat diagram, explain operation mode and privilege levels in cortex M3. **(08 Marks)**

OR

2 a. What is stack? Explain push and pop operation. With the help of a neat diagram. **(07 Marks)**
b. Explain in detail special registers used in ARM cortex M3 processor. **(09 Marks)**

Module-2

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b. Explain the following instruction set : i) BFC ii) SBFX iii)ASR iv) MRS. **(04 Marks)**
c. Explain how CMSIS provides standard access. Interface for Embedded software. **(04 Marks)**

OR

4 a. Write a program to blink a LED using 'C' language. **(08 Marks)**
b. Explain the following assembler directives AREA, ENTRY, DCB, ALIGN. **(04 Marks)**
c. Explain different bus interfaces supported by cortex M3. **(04 Marks)**

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5 a. Explain how embedded system are classified. **(08 marks)**
b. With neat block diagram, explain the element of embedded system. **(08 Marks)**

OR

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c. Explain how brown-out protection circuits works. **(04 Marks)**

Module-4

7 a. What are the operational and nonoperational attributes of an embedded systems. **(10 Marks)**
b. Explain different types of serial interface bus used in automotive communication. **(06 Marks)**

OR

8 a. Explain fundamental issues in hardware software co-design. **(06 Marks)**
b. Explain with a neat block diagram how source file to object file translation take place. **(06 marks)**
c. Explain super loop based approach of embedded firmware design. **(04 Marks)**

CBCS SCHEME

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15EC62

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
ARM Microcontroller and Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain architectural features of cortex M3 with block diagram. **(07 Marks)**
b. Briefly describe the special registers of cortex M3. **(06 Marks)**
c. What is stack and what are the instructions to access stack? **(03 Marks)**

OR

2 a. Briefly discuss features of built in nested vector interrupt controller. **(08 Marks)**
b. Write a short note on :
i) Debugging support
ii) Interrupts and exceptions supported by cortex M3. **(08 Marks)**

Module-2

3 a. Explain memory map of cortex M3 with diagram. **(08 Marks)**
b. Write C language program to toggle an LED with small delay in cortex M3. **(05 Marks)**
c. Explain the 32 bit multiply instruction set. **(03 Marks)**

OR

4 a. Explain arithmetic instruction set with example. **(07 Marks)**
b. Briefly explain shift and rotate instructions with diagrams. **(07 Marks)**
c. Explain working of following instructions :
i) CMP ii) TST iii) CMN iv) REV. **(02 Marks)**

Module-3

5 a. Explain the sequence of operations for communicating with an I2C slave device. **(08 Marks)**
b. Write the differences between :
i) RISC and CISC
ii) Harvard architecture and Von Neumann architecture. **(08 Marks)**

OR

6 a. Briefly explain PLDs and types of PLDs. **(06 Marks)**
b. Write short note on :
i) Optocoupler
ii) COTS. **(08 Marks)**
c. Explain working of DRAM. **(02 Marks)**

CBCS Scheme

USN | | | | | | | | | |

15EC62

Sixth Semester B.E. Degree Examination, June/July 2018
ARM Microcontroller & Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: *Answer FIVE full questions, choosing one full question from each module.*

Module-1

1 a. With a neat diagram, explain the architecture of ARM cortex M3 microcontroller. **(10 Marks)**

b. Explain the register organization of Cortex M3. **(06 Marks)**

OR

2 a. Explain the operation modes and privilege levels available in ARM cortex M3 with a neat transition diagram. **(06 Marks)**

b. Mention the instructions used for accessing the special registers. Explain the same using suitable examples. **(04 Marks)**

c. Explain the stack operations using Push and Pop instructions in ARM Cortex M3. **(06 Marks)**

Module-2

3 a. Explain shift and Rotate instructions available in ARM Cortex M3 instruction set. Why is there rotate right instruction but no rotate left instruction in Cortex M3? **(08 Marks)**

b. Explain the following instructions with suitable example:
(i) BFC (ii) SXTH (iii) UBFX (iv) RBIT **(08 Marks)**

OR

4 a. Write the memory map and explain memory access attributes in Cortex M3. **(08 Marks)**

b. Analyse the following instructions and write the contents of the registers after the execution of each instruction:
Assume R8 = 0x00000088, R9 = 0x00000006 and R3 = 0x00001111
(i) RSB.W R8, R9, #0x10
(ii) ADD R8, R9, R3
(iii) BIC.W R6, R8, #0x06
(iv) ORR R8, R9 **(08 Marks)**

Module-3

5 a. Differentiate between:
(i) RISC and CISC architecture.
(ii) Little Endian and Big Endian architecture. **(08 Marks)**

b. What are the features of the following:
(i) I2C bus
(ii) IrDA
(iii) Optocoupler
(iv) 1-wire interface **(08 Marks)**

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Academic Calendar of VTU, Belagavi for EVEN Semester of 2018-2019 (Feb 2018 – July 2019)

	II Sem B. E. / B. Tech. / B. Arch	IV & VI Sem B. E. /B. Tech. IV, VI,VIII Sem B. Arch.	VIII Sem B.E / B.Tech & X Sem B. Arch	IV Sem MCA	VI Sem MCA	IV Sem MBA	IV Sem M. Tech.	IV Sem M. Arch.	II Sem M. Tech.	II Sem MCA	II Sem MBA	II Sem M. Arch.
Commencement of EVEN Semester	25.02.2019	01.02.2019	01.02.2019	01.02.2019	01.02.2019	18.02.2019	28.12.2018	01.02.2019	01.03.2019	01.03.2019	25.02.2019	25.02.2019
Last Working day of EVEN Semester	17.06.2019	23.05.2019	23.05.2019	18.05.2019	18.05.2019	01.06.2019	13.04.2019	18.05.2019	21.06.2019	21.06.2019	17.06.2019	17.06.2019
Practical Examination	19.06.2019 To 29.06.2019	27.05.2019 To 07.06.2019	-	21.05.2019 To 25.05.2019	-	-	-	-	24.06.2019 To 29.06.2019	24.06.2019 To 29.06.2019	-	-
Theory Examinations	01.07.2019 To 16.07.2019	10.06.2019 To 16.07.2019	27.05.2019 To 07.06.2019	27.05.2019 To 15.06.2019	-	03.06.2019 To 28.06.2019	27.05.2019 To 31.05.2019	-	01.07.2019 To 12.07.2019	01.07.2019 To 12.07.2019	20.06.2019 To 04.07.2019	20.06.2019 To 04.07.2019
Viva Voce		-	11.06.2019 To 17.06.2019	-	-	-	-	-	-	-	-	-
Summer Project / Professional training /	-	-	-	-	20.05.2019 To 29.05.2019 [Submission of report to VTU]	01.04.2019 To 15.04.2019 [Submission of report to VTU]	03.06.2019 To 18.06.2019 [Submission of report to VTU]	-	-	-	-	-
Commencement of ODD Semester	22.07.2019	22.07.2019	-	22.07.2019	-	-	-	-	22.07.2019	22.07.2019	22.07.2019	22.07.2019

NOTE

1. College Time Table shall be arranged for five and a half week days and planned to accommodate EDUSAT transmission slots, the schedule of which will be notified separately.
2. The faculty/staff shall be available to undertake any work assigned by the university.
3. If any of the above date is declared to be a holiday then the corresponding event will come into effect on the next working day.
4. Notification regarding Calendar of Events relating to the conduct of University Examination will be issued by the Registrar (Evaluation) from time to time

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REGISTRAR

Sapthagiri College of Engineering

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Calendar of Events

AY:2018-2019

Sem: IV,VI & VIII

	Mon	Tue	Wed	Thru	Fri	Sat	Events
Feb					1	2	1: Commencement of Even Semester 23 : Alumni meet 16 : Proctors report
	4	5	6	7	8	9	
	11	12	13	14	15	16	
	18	19	20	21	22	23	
	25	26	27	28			
Mar					1	2	4 : Mahashivaratri 5 : Monthly attendance report 6 : Proctors report 11 - 13: First IA test 20 : Proctor report 29 - 30 : SANKALP - 19
	4	5	6	7	8	9	
	11	12	13	14	15	16	
	18	19	20	21	22	23	
	25	26	27	28	29	30	
Apr	1	2	3	4	5	6	6 : Ugadi 8 : Monthly attendance report 10 : Proctor report 15 - 17: Second IA test 24 : Proctor report
	8	9	10	11	12	13	
	15	16	17	18	19	20	
	22	23	24	25	26	27	
	29	30					
May			1	2	3	4	1 : May Day 6 : Monthly attendance report 11 - Graduation Day 16 - 18: Third IAI test 20 - 22: Lab IA test 24 : Proctor report 23 :Last working day 27/05/19 – 07/06/19:Theory exams (8th Sem) 27/05/19 – 07/06/19: Lab exams (4th & 6th Sem)
	6	7	8	9	10	11	
	13	14	15	16	17	18	
	20	21	22	23	24	25	
	27	28	29	30	31		
June						1	5 : Ramzan 11/06/19 – 17/06/19: Viva Voce (8th Sem) 10/06/19 - 16/07/19 :Theory exams (4th & 6th Sem)
	3	4	5	6	7	8	
	10	11	12	13	14	15	
	17	18	19	20	21	22	
	24	25	26	27	28	29	

Commencement of ODD semester for AY 2019-20: 22 July 2019

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Calendar of Events

AY: 208-19 | **Sem: II**

	Mon	Tue	Wed	Thru	Fri	Sat	Events
Feb					1	2	23 : Alumni meet 25 : Commencement of Even Semester
	4	5	6	7	8	9	
	11	12	13	14	15	16	
	18	19	20	21	22	23	
	25	26	27	28			
Mar					1	2	4 : Mahashivaratri 16 : Proctor report 29 - 30 : SANKALP 2019
	4	5	6	7	8	9	
	11	12	13	14	15	16	
	18	19	20	21	22	23	
	25	26	27	28	29	30	
Apr	1	2	3	4	5	6	6 :Ugadi 5 : Proctor report 8 :Monthly attendance report 15 - 17 : First IA test 24 - Proctor report
	8	9	10	11	12	13	
	15	16	17	18	19	20	
	22	23	24	25	26	27	
	29	30					
May			1	2	3	4	1 : May Day 6 :Monthly attendance report 10 - Proctor report 11 : Graduation Day 16 - 18 : Second IA test 22 : Proctor report
	6	7	8	9	10	11	
	13	14	15	16	17	18	
	20	21	22	23	24	25	
	27	28	29	30	31		
June						1	3 - 8 : Lab IA test 5 : Ramzan 10 - 12 : Third IA test 10 : Monthly attendance report 15 : Proctor report 17 : Last working day 19 – 29th June : VTU Practical Exams 1 – 16th July : VTU Theory
	3	4	5	6	7	8	
	10	11	12	13	14	15	
	17	18	19	20	21	22	
	24	25	26	27	28	29	

Commencement of ODD semester for AY 2019-20: 22 July 2019

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018–19 (EVEN) **with effect from: 01-02-2019**

INDIVIDUAL TIME TABLE

Semester: VI (A & B) **Staff Name: Prof. AGALYA P**

Subject: ARM Microcontroller & Embedded Systems **Subject Code: 15EC62**

Time / Day	8:30 - 9:30	9:30 - 10:30	BREAK 10:30 - 10:50	10:50 - 11:50	11:50 - 12:50	12:50 - 1:45	1:45 - 2:40	2:40 - 3:35	3:35 - 4:30
MON	A					LUNCH BREAK	EM LAB 15ECL-67(A-1)		
TUE		A			B				
WED	EM LAB 15ECL-67(B-3)							B	
THU		B			A				
FRI		A		B					
SAT									

Signature of Staff

Signature of Coordinator

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Signature of HOD 8/4/19

SAPTHAGIRI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION

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ODD SEMESTER TIME-TABLE WITH EFFECT FROM 01/02/2019

DEPARTMENT/BRANCH	ECE	SEMESTER: VI	SECTION: B
ACADEMIC YEAR	2018-19	ROOM NO	311
CLASS TEACHER	PROF. VINAY H C		

PROCTOR: PROF. SHOBHA H MOBILE: 8123538587 EMAIL:shobha_hugar@yahoo.co.in	PROCTOR: PROF. VINAY H C MOBILE: 8792526968 EMAIL:vinnuhc@gmail.com	PROCTOR: PROF. T SWAMY MOBILE: 7353591676 EMAIL:thippeswamy35@gmail.com

BREAK	1	2	BREAK	3	4	BREAK	5	6	7
TIME	8:30AM - 9:30AM	9:30AM - 10:30AM	10:30AM - 10:50AM	10:50AM - 11:50AM	11:50AM - 12:50PM	12:50PM - 01:45PM	01:45PM - 02:40PM	02:40PM - 03:35PM	03:35PM - 04:30PM
DAY									
MON	DC	VLSI		DSDV	DSS	LUNCH BREAK	TUTORIALS		
TUE	VLSI	DC		CCN	AME		DSS(TT)	DSDV(TT)	EDUSAT
WED	EM LAB 15ECL-67(B-3)/CCN LAB 15ECL68(B-1)				VLSI		DC	AME	TUTORIAL
THU	DSDV	AME		CCN	DC		EM LAB 15ECL-67(B-1)/CCN LAB 15ECL68(B-2)		
FRI	CCN	DSS		AME	DSDV		EM LAB 15ECL-67(B-2)/CCN LAB 15ECL68(B-3)		
SAT	DSS	CCN		VLSI	FORUM ACTIVITY				

SUBJECTS ALLOCATION

SUBJECT CODE	SUBJECT TITLE	FACULTY NAME	FACULTY CODE
15EC61	Digital Communication	PROF. VINAY H C	VHC
15EC62	ARM Microcontroller & Embedded Systems	PROF. AGALYA S	AP
15EC63	VLSI Design	PROF.SHOBHA H	SH
15EC64	Computer Communication Networks	PROF. T.YADAV	TY
15EC654	Professional Elective-2- Digital Switching Systems	PROF. SUMA V SHETTY	SVS
15EEC663	Open Elective-2-Digital System Design using Verilog	PROF. VANI A	VA
15ECL67	Embedded Controller Lab	B1-PROF. SHOBHA S PROF. PREETHI T S B2-PROF. PREETHI T S, PROF. SHWETHA G B3-PROF. AGALYA P, PROF. KARTHIK N C	SS, PTS PTS, SG AP, KNC
15ECL68	Computer Networks Lab	B1-PROF. THIPPESWAMY E, PROF. VINAY H C B2-PROF. SUDHA M S, PROF. VANI V B3- PROF. SUDHA M S, PROF. VANI V	TS, VHC SMS, VV SMS, VV

TIME TABLE COORDINATOR

(S K MURTHY)
HOD
31.1.19

31/1

PRINCIPAL

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SAPTHAGIRI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION

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ODD SEMESTER TIME-TABLE WITH EFFECT FROM 01/02/2019

DEPARTMENT/BRANCH	ECE	SEMESTER: VI	SECTION: A
ACADEMIC YEAR	2018-19	ROOM NO:	309
CLASS TEACHER	PROF. T YADAV G		

PROCTOR: PROF. PREETHI T S, T YADAV G
MOBILE: 9742844413, 9743244344
EMAIL:ts.preethi@gmail.com
thimrajyadav@gmail.com

PROCTOR: PROF. RAVISHANKAR, SUDHA M S
MOBILE: 9916592006, 9480616926
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Sudhams28@yahoo.com

BREAK	1	2	BREAK	3	4	BREAK	5	6	7
TIME	8:30AM - 9:30AM	9:30AM - 10:30AM	10:30AM - 10:50AM	10:50AM - 11:50AM	11:50AM - 12:50PM	12:50PM - 01:45PM	01:45PM - 02:40PM	02:40PM - 03:35PM	03:35PM - 04:30PM
DAY									
MON	AME	DSS		DC	CCN		EM LAB 15ECL-67(A-1)/CCN LAB 15ECL68(A-2)		
TUE	DC	AME		VLSI	DSDV(TT)		EM LAB 15ECL-67(A-2)/CCN LAB 15ECL68(A-3)		
WED	CCN	VLSI		DC	DSS	LUNCH BREAK	EM LAB 15ECL-67(A-3)/CCN LAB 15ECL68(A-1)		
THU	DSS	DC		DSDV	AME		DSS(TT)	TUTORIAL	EDUSAT
FRI	DSDV	AME		VLSI	CCN		TUTORIAL		
SAT	VLSI	DSDV		CCN	FORUM ACTIVITY				

SUBJECTS ALLOCATION

SUBJECT CODE	SUBJECT TITLE	FACULTY NAME	FACULTY CODE
15EC61	Digital Communication	PROF. SANDHYA RANI M H	SMH
15EC62	ARM Microcontroller & Embedded Systems	PROF. AGALYA P	AP
15EC63	VLSI Design	PROF.SHOBHA H	SH
15EC64	Computer Communication Networks	PROF. T.YADAV	TY
15EC654	Professional Elective-2- Digital Switching Systems	PROF. SUMA V SHETTY	SVS
15EEC663	Open Elective-2-Digital System Design using Verilog	PROF. VANI A	VA
15ECL67	Embedded Controller Lab	A1-PROF. AGALYA P, PROF. KARTHIK N C A2-PROF. PREETHI T S, PROF. VINAY H C A3-PROF. SHOBHA S, PROF. KARTHIK N C	AP, KNC PTS, VHC SS, KNC
15ECL68	Computer Networks Lab	A1-PROF. THIPPESWAMY E, PROF. T YADAV A2-PROF. VINAY H C, PROF.T YADAV A3- PROF. THIPPESWAMY E, PROF. T YADAV	TS, TY VHC, TY TS, TY

TIME TABLE COORDINATOR

CS K MURTHY
HOD
31/1/19

PRINCIPAL

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SAPTHAGIRI COLLEGE OF ENGINEERING
LESSON PLAN FOR THE ACADEMIC YEAR: EVEN 2018-19

Course	ARM Microcontroller and Embedded System				Course code		15EC62
Faculty	P. Agalya				Semester/Sec		6/A
Core/Elective	Contact Hours /week			Total Hours	Assessment		Credits
Core	L	T	P	50	CIE	SEE	4
	4	-	-		20	80	
Prerequisites	1. Number System 2. Digital Electronics, Digital Integrated circuits 3. Microprocessor, Microcontroller Fundamentals						

Course Objectives

1	Understand the architectural features and different instruction set of 32 bit ARM Cortex M3 processor core.
2	Program ARM Cortex M3 using assembly level instructions and C language for different applications.
3	Understand the basic hardware components of an embedded system and their selection method based on the characteristics and quality attributes.
4	Develop the hardware software co-design and firmware design approaches.
5	Explain the need of real time operating system for embedded system applications.

Syllabus	
MODULE 1	**RBT Level**
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence. (Text 1: Ch 1, 2, 3)	**L1, L2**
MODULE 2	
ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, useful instructions, Assembly and C language Programming. (Text 1: Ch-4, Ch-5, Ch-10 (10.1, 10.2, 10.3, 10.5 only)).	**L1, L2**
MODULE 3	
Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Core of an Embedded System including all types of processor/controller, Memory, Sensors, Actuators, LED, 7 segment LED display, Optocoupler, relay, Piezo buzzer, Push button switch, Communication Interface	**L1,L2, L3**

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(onboard and external types), Embedded firmware, Other system components. (Text 2: All the Topics from Ch-2 & 3, excluding 2.3 & 3.4 (stepper motor), 2.3 & 3.8 (keyboard) and 2.3 & 3.9 (PPI) sections).	
MODULE 4	
Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling (excluding UML), Embedded firmware design and development (excluding C language). (Text 2: Ch-3, Ch-4, Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)	**L1, L2, L3**
MODULE 5	
RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques (Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch 12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)	**L1,L2,L3**

Text Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009.

Course outcomes

At the end of this course the students will be able

CO1	To describe the architectural features and instruction set architecture of 32 bit ARM Cortex M3 processor core.
CO2	To describe the memory map of cortex m3 and apply the knowledge gained for Programming ARM Cortex M3 for different applications.
CO3	To apply the knowledge in selecting basic hardware components in the design of embedded system based on the characteristics and attributes of an embedded system.
CO4	To describe the development of an embedded system using the hardware /software co-design and firmware design approaches.
CO5	To explain the need of real time operating system for embedded system applications.

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SAPTHAGIRI COLLEGE OF ENGINEERING
LESSON PLAN FOR THE ACADEMIC YEAR: EVEN 2018-19

Lesson plan

Period	Date	Topic Planned	Actual Date	Topics Covered	Remarks
1.	1/2/19	**ARM-32 bit Microcontroller:** Introduction to Thumb-2 technology and applications of ARM.	4/2/19	Introduction to ARM Microcontrollers & ISA.	Students started attending the class only from 4th feb.
2.	4/2/19	Architecture of ARM Cortex M3	5/2/19	Thumb2 ISA & Applications of ARM	
3.	5/2/19	Architecture of ARM Cortex M3, Various Units in the architecture,	7/2/19	Architecture of ARM cortex M3.	
4.	7/2/19	Debugging support, General Purpose Registers	8/2/19	General purpose Registers & special Registers.	
5.	8/2/19	Special Registers of Cortex M3	11/2/19	Special Registers of cortex M3, & NVIC, & operating modes.	
6.	11/2/19	Exceptions of Cortex M3	12/2/19	Exceptions & Interrupts of Cortex M3.	
7.	12/2/19	Interrupts of Cortex M3	18/2/19	Exceptions & Interrupts handling & Stack operations	placement & training from 13th feb to 15th feb.
8.	14/2/19	Stack operation of Cortex M3	19/2/19	Stack model of cortex M3 with operations.	

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9.	15/2/19	Reset sequence of Cortex M3	20/2/19	Debug Support of Cortex M3 Reset sequence.	
10.	18/2/19	Revision and discussion of Module 1 university QP.	21/2/19	Revision & Module 1 QP discussion.	
At the end of this topic the students will be able to describe the architectural features and instruction set architecture of 32 bit ARM Cortex M3 processor core.					
11.	19/2/19	**ARM Cortex M3 Instruction Sets and Programming:** Assembly basics	~~L1, L2~> 25/2/19	Assembly basics.	
12.	21/2/19	Instruction list and description, Data processing instructions – 16bit & 32bit	26/2/19	Data transfer instructions MOV, MVN, LDR	
13.	22/2/19	Data processing instructions – 16bit & 32bit	28/2/19	Load & store instructions 16bit & 32bit.	
14.	25/2/19	Load & Store instructions – 16 & 32bit	1/3/19	Data processing instructions. Add, Sub, MUL & DIV	
15.	26/2/19	Load & Store instructions – 16 & 32bit	5/3/19	logical operations AND, OR, ORN, EOR, shift & Rotate operations.	
16.	28/2/19	Branch instructions	7/3/19	Branch instructions.	
17.	1/3/19	Useful instructions of ARM Cortex M3	8/3/19	Useful instructions of ARM cortex M3.	
18.	5/3/19	Assembly programming	14/3/19	Assembly programming.	

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19.	7/3/19	C Language Programming using Cortex M3	14/3/19	C Language programming using cortex M3.	
20.	8/3/19	C Language Programming using Cortex M3	18/3/19	Revision of University QP.	
At the end of this topic the students will be able to describe the memory map of cortex m3 and apply the knowledge gained for Programming ARM Cortex M3 for different applications.					
21.	11/3/19	**Embedded System Components:** Embedded Vs General computing system, Classification of Embedded systems	19/3/19	Embedded s/m components. Embedded Vs GPS, Von-neumann Vs Harvard, RISC Vs CISC, classification.	
22.	14/3/19	Major applications and purpose of ES.	26/3/19	Applications & purpose of Embedded s/m.	
23.	15/3/19	Core of an Embedded System including all types of processor/controller	1/4/19	Core of an Embedded s/m	
24.	18/3/19	Memory, Sensors, Push button switch	2/4/19	Memory. RAM & Rom types & its importance in ES.	
25.	19/3/19	Actuators, LED, 7 segment LED display	5/4/19	Sensors, Push button, Switch, Actuators.	
26.	21/3/19	Optocoupler, relay, Piezo buzzer	8/4/19	LED, 7 Segment LED, Relay, opto-coupler, piezobuzzer.	
27.	22/3/19	Communication Interface (onboard and external types)	10/4/19	Communication Interface - onboard I^2C, SPI, UART	

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28.	25/3/19.	Embedded firmware	4/4/19	Communication Interface, entering USB, RS232, Bluetooth Zigbee, wifi etc.	
29.	26/3/19	Other system components.	19/4/19	Embedded firmware, Reset Circuit.	
30.	28/3/19	Discussion of University QP	23/4/19	Watch dog timer, Brownout protection Circuit. University Qp discussion.	
At the end of this topic the students will be able to apply the knowledge in selecting basic hardware components in the design of embedded system based on the characteristics and attributes of an embedded system.					
31.	1/4/19.	**Embedded System Design Concepts:** Characteristics of Embedded system	25/4/19	Characteristics of Embedded system	
32.	2/4/19.	Quality Attributes of Embedded Systems	26/4/19	Quality attributes of Embedded s/m.	
33.	4/4/19.	Operational and non-operational quality attributes of embedded system.	29/4/19	Operational & Quality attributes.	
34.	5/4/19.	Embedded Systems-Application and Domain specific	30/4/19	Non operational Quality attributes.	
35.	8/4/19.	Embedded Systems-Application and Domain specific	2/5/19	Application & domain specific Embedded s/m.	
36.	9/4/19.	Hardware Software Co-Design	3/5/19	Hardware Software co-design.	

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37.	11/4/19	Program Modelling (excluding UML)	6/5/19	Program modeling Embedded firmware design.	
38.	12/4/19	Embedded firmware design and development (excluding C language).	7/5/19	Embedded firmware design.	
39.	18/4/19	Embedded firmware design and development (excluding C language).	9/5/19	Embedded firmware development.	
40.	19/4/19	Discussion of university QP.	10/5/19	Discussion on university QP.	
At the end of this topic the students will be able to describe the development of an embedded system using the hardware /software co-design and firmware design approaches.					
41.	22/4/19	RTOS and IDE for Embedded System Design: Operating System basics	13/5/19	RTOS & IDE for Embedded s/m design.	
42.	23/4/19	Types of operating systems	14/5/19	Types of operating s/m.	
43.	25/4/19	Task, process and threads (Only POSIX Threads with an example program)	14/5/19.	Task process threads, posix threads with example.	
44.	26/4/19	Thread preemption, Preemptive Task scheduling techniques	15/5/19.	preemptive task scheduling.	
45.	29/4/19	Task Communication	15/5/19.	Task communi-cation, pipe, mailbox,	
46.	30/4/19	Task synchronization issues – Racing and Deadlock	20/5/19	shared Memory, message queue implementation.	

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47.	21/5/19	Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS	21/5/19.	Task synchro-nization Racing & deadlock.	
48.	8/5/19	Integration and testing of Embedded hardware and firmware	23/5/19		
49.	6/5/19	Embedded system Development Environment – Block diagram (excluding Keil)	23/5/19.		
50.	7/5/19.	Disassembler/decompiler, simulator, emulator and debugging techniques			
At the end of this topic the students will be able to explain the need of real time operating system for embedded system applications.					

PROGRAMME OUTCOMES

Program outcomes are narrower statements that describe what students are expected to know and be able to do by the time of graduation. These relate to the skills, knowledge and behavior. Graduation students of **Bachelor of Electronics & Communication Engineering** program at Sapthagiri College of Engineering will attain the following program outcomes **in the field of Electronics & Communication engineering.**

	PROGRAM OUTCOME
PO1.	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2.	**Problem analysis**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3.	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4.	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5.	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern

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	engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
PO6.	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7.	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8.	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9.	**Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10.	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11.	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12.	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAMME SPECIFIC OUTCOMES

At the end of the B.E Electronics & Communication Engineering program, students of sapthagiri college of Engineering are expected to have developed the following program specific outcomes.

	PROGRAM SPECIFIC OUTCOMES
PSO1	Specify, design, build and test analog, digital and embedded systems for signal processing
PSO2	Understand and architect wired and wireless analog and digital communication systems as per specifications, and determine their performance.

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CO-PO Mapping

Mapping of Course outcomes, Program Objectives and Program specific outcomes
Note: 1 = Slight 2 = Moderate 3 = Strong

Course outcomes	Program Outcomes												PSOs		Total
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	
CO-1	3	0	3										3	0	
CO-2	3	2	2										3	0	
CO-3	3	0	2										3	0	
CO-4	3	0	1										3	3	
CO-5	3	2	3										3	0	
Average	3	0.8	2.2										3	0.6	

Signature of Principal **Signature of HOD** **Signature of faculty**

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
SAPTHAGIRI COLLEGE OF ENGINEERING
LESSON PLAN FOR THE ACADEMIC YEAR: EVEN 2018-19
(Faculty)

Course	ARM Microcontroller and Embedded System				Course code		15EC62
Faculty	P. Agalya				Semester/Sec		6/B
Core/Elective	Contact Hours /week			Total Hours	Assessment		Credits
Core	L	T	P	50	CIE	SEE	4
	4	-	-		20	80	
Prerequisites	1. Number System 2. Digital Electronics, Digital Integrated circuits 3. Microprocessor, Microcontroller Fundamentals						

Course Objectives	
1	Understand the architectural features and instruction set of 32 bit microcontroller ARM Cortex M3.
2	Program ARM Cortex M3 using assembly level instructions and C language for different applications.
3	Understand the basic hardware components of an embedded system and their selection method based on the characteristics and quality attributes.
4	Develop the hardware software co-design and firmware design approaches.
5	Explain the need of real time operating system for embedded system applications.

Syllabus	
MODULE 1	RBT Level
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence. (Text 1: Ch 1, 2, 3)	L1, L2
MODULE 2	
ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, useful instructions, Assembly and C language Programming. (Text 1: Ch-4, Ch-5, Ch-10 (10.1, 10.2, 10.3, 10.5 only)).	L1, L2
MODULE 3	
Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Core of an Embedded System including all types of processor/controller, Memory, Sensors, Actuators, LED, 7 segment LED display, Optocoupler, relay, Piezo buzzer, Push button switch, Communication Interface	L1,L2, L3

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(onboard and external types), Embedded firmware, Other system components. (Text 2: All the Topics from Ch-2 & 3, excluding 2.3 & 3.4 (stepper motor), 2.3 & 3.8 (keyboard) and 2.3 & 3.9 (PPI) sections).	
MODULE 4	
Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling (excluding UML), Embedded firmware design and development (excluding C language). (Text 2: Ch-3, Ch-4, Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)	**L1, L2, L3**
MODULE 5	
RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques (Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch 12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)	**L1,L2,L3**

Text Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009.

Course outcomes	
At the end of this course the students will be able	
CO1	To describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
CO2	To describe the memory map of cortex m3 and apply the knowledge gained for Programming ARM Cortex M3 for different applications.
CO3	To apply the knowledge in selecting basic hardware components in the design of embedded system based on the characteristics and attributes of an embedded system.
CO4	To describe the development of an embedded system using the hardware /software co-design and firmware design approaches.
CO5	To explain the need of real time operating system for embedded system applications.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SAPTHAGIRI COLLEGE OF ENGINEERING

LESSON PLAN FOR THE ACADEMIC YEAR: EVEN 2018-19

(Faculty)

Lesson plan

Period	Date	Topic Planned	Actual Date	Topics Covered	Remarks
1.	1/2/19	**ARM-32 bit Microcontroller:** Introduction to Thumb-2 technology and applications of ARM.	5/2/19	Introduction to ARM Mc & ISR.	students started attending for 5/2/19.
2.	5/2/19	Architecture of ARM Cortex M3	7/2/19	Thumb2 ISA & Application	
3.	6/2/19	Architecture of ARM Cortex M3, Various Units in the architecture,	8/2/19	Architecture of ARM cortex M3 Gppp Registers.	
4.	8/2/19.	Debugging support, General Purpose Registers	12/2/19	Special purpose registers. PSR, Mask registers.	
5.	12/2/19.	Special Registers of Cortex M3	19/2/19	CONTROL Registers. operating modes	placement & training from 13th feb to 15th feb.
6.	13/2/19.	Exceptions of Cortex M3	20/2/19	NVIC, Exceptions & interupts of Cortex M3.	
7.	14/2/19	Interrupts of Cortex M3	22/2/19	Exceptions & interupts Handling.	
8.	15/2/19.	Stack operation of Cortex M3	26/2/19.	Stack operations of Cortex M3	

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9.	18/2/19	Reset sequence of Cortex M3	27/2/19	Stack Model, Debug support of cortex M3.	
10.	20/2/19	Revision and discussion of Module 1 university QP.	28/2/19	Reset sequence Revision of Module 1.	
At the end of this topic the students will be able to describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.					
11.	21/2/19	**ARM Cortex M3 Instruction Sets and Programming:** Assembly basics	1/3/19	Assembler basics, Data transfer instructions Introduction	
12.	22/2/19	Instruction list and description, Data processing instructions – 16bit & 32bit	5/3/19	Data transfer instructions MOV, MVN,	
13.	26/2/19	Data processing instructions – 16bit & 32bit	6/3/19	load & store instructions LDR & STR.	
14.	27/2/19	Load & Store instructions – 16 & 32bit	7/3/19	Data processing instruction Add, Sub, MUL & DIV	
15.	28/2/19	Load & Store instructions – 16 & 32bit	8/3/19	Logical operations AND, OR, ORN EOR, shift & rotate operations.	
16.	11/3/19	Branch instructions	14/3/19	Branch instructions.	
17.	5/3/19	Useful instructions of ARM Cortex M3	15/3/19	Useful instructions of Cortex-M3.	
18.	6/3/19	Assembly programming	19/3/19	Assembly programming	

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19.	7/3/19	C Language Programming using Cortex M3	20/3/19	C Language programming using cortex-M3	
20.	8/3/19	C Language Programming using Cortex M3	26/3/19	Revision of University Qp.	
At the end of this topic the students will be able to describe the memory map of cortex m3 and apply the knowledge gained for Programming ARM Cortex M3 for different applications.					
21.	14/3/19	**Embedded System Components:** Embedded Vs General computing system, Classification of Embedded systems	2/4/19	Embedded s/m components, Embedded Vs General purpose system, Harvard & Von-neumann, RISC & CISC.	
22.	19/3/19	Major applications and purpose of ES.	3/4/19	Applications & purpose of Embedded s/m.	
23.	20/3/19	Core of an Embedded System including all types of processor/controller	5/4/19	Core of an Embedded s/m.	
24.	21/3/19	Memory, Sensors, Push button switch	9/4/19	Memory RAMs & ROM types, importance of ES.	
25.	22/3/19	Actuators, LED, 7 segment LED display	10/4/19	Sensors, push button, switch, Actuators	
26.	26/3/19	Optocoupler, relay, Piezo buzzer	11/4/19	LED, 7 Segment LED, Relay, opto coupler, piezo buzzer.	
27.	27/3/19	Communication Interface (onboard and external types)	12/4/19	Communication Interface onboard I^2C & SPI & UART	

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28.	28/3/19	Embedded firmware	9/4/19	Communication interface external RS232, USB, Bluetooth, Zigbee	
29.	29/3/19	Other system components.	23/4/19	Embedded firmware, Reset Circuit.	
30.	2/4/19.	Discussion of University QP	24/4/19.	Watch dog circuit, Brownout protection Circuit, Discussion of University QP.	
At the end of this topic the students will be able to apply the knowledge in selecting basic hardware components in the design of embedded system based on the characteristics and attributes of an embedded system.					
31.	3/4/19	**Embedded System Design Concepts:** Characteristics of Embedded system	25/4/19	Characteristics of Embedded s/m.	
32.	4/4/19	Quality Attributes of Embedded Systems	30/4/19	Quality attributes of Embedded s/m.	
33.	5/4/19	Operational and non-operational quality attributes of embedded system.	2/5/19	operational Quality attributes	
34.	9/4/19	Embedded Systems-Application and Domain specific	3/5/19	Non operational Quality attributes.	
35.	10/4/19	Embedded Systems-Application and Domain specific	7/5/19	Application & domain specific ES.	
36.	11/4/19	Hardware Software Co-Design	8/5/19.	Hardware software co-design.	
37.	12/4/19.	Program Modelling (excluding UML)	9/5/19.	program modeling.	

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SAPTHAGIRI COLLEGE OF ENGINEERING

LESSON PLAN FOR THE ACADEMIC YEAR: EVEN 2018-19

(Faculty)

38.	12/4/19	Embedded firmware design and development (excluding C language).	13/5/19	Program modeling & Embedded firmware	
39.	19/4/19	Embedded firmware design and development (excluding C language).	13/5/19	Embedded firmware development	
40.	23/4/19	Discussion of university QP.	17/5/19	Discussion of university QP.	
At the end of this topic the students will be able to describe the development of an embedded system using the hardware /software co-design and firmware design approaches.					
41.	24/4/19	RTOS and IDE for Embedded System Design: Operating System basics	14/5/19	RTOS, IDE for Embedded Sys.	
42.	25/4/19	Types of operating systems	14/5/19	OS basics & types	
43.	26/4/19	Task, process and threads (Only POSIX Threads with an example program)	20/5/19	Task, process, threads, POSIX THREADS.	
44.	30/4/19	Thread preemption, Preemptive Task scheduling techniques	20/5/19	pre-emptive task scheduling.	
45.	2/5/19	Task Communication	21/5/19	Task Communi-cation pipe, mailbox.	
46.	3/5/19	Task synchronization issues – Racing and Deadlock	22/5/19	Task comm. Shared memory, message queue implementation.	
47.	7/5/19	Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS	23/5/19	Task Synchronisation Racing & Deadlock.	

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48.	31.5.19	Integration and testing of Embedded hardware and firmware			
49.	9.5.19	Embedded system Development Environment – Block diagram (excluding Keil)			
50.	10.5.19	Disassembler/decompiler, simulator, emulator and debugging techniques			
At the end of this topic the students will be able to explain the need of real time operating system for embedded system applications.					

PROGRAMME OUTCOMES

Program outcomes are narrower statements that describe what students are expected to know and be able to do by the time of graduation. These relate to the skills, knowledge and behavior. Graduation students of **Bachelor of Electronics & Communication Engineering** program at Sapthagiri College of Engineering will attain the following program outcomes **in the field of Electronics & Communication engineering.**

	PROGRAM OUTCOME
PO1.	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2.	**Problem analysis**: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3.	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4.	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5.	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
PO6.	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

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PO7.	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8.	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9.	**Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10.	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11.	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12.	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAMME SPECIFIC OUTCOMES

At the end of the B.E Electronics & Communication Engineering program, students of sapthagiri college of Engineering are expected to have developed the following program specific outcomes.

	PROGRAM SPECIFIC OUTCOMES
PSO1	Specify, design, build and test analog, digital and embedded systems for signal processing
PSO2	Understand and architect wired and wireless analog and digital communication systems as per specifications, and determine their performance.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SAPTHAGIRI COLLEGE OF ENGINEERING

LESSON PLAN FOR THE ACADEMIC YEAR: EVEN 2018-19

(Faculty)

CO-PO Mapping

Mapping of Course outcomes, Program Objectives and Program specific outcomes

Note: 1 = Slight 2 = Moderate 3 = Strong

Course outcomes	Program Outcomes												PSOs		Total
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	
CO-1	3	0	3										3	0	
CO-2	3	2	2										3	0	
CO-3	3	0	2										3	0	
CO-4	3	0	1										3	3	
CO-5	3	2	3										3	0	
Average	3	0.8	2.2										3	0.6	

Signature of Principal Signature of HOD Signature of faculty

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Sapthagiri College of Engineering
Department of Electronics and Communication Engineering
Students Name List

Semester: 6th 'A' **Academic Year: 2018–19**

Sl. No.	USN	Name of the student
1.	1SG15EC017	ASHWIN V
2.	1SG15EC056	MANJUNATHA NAIK N
3.	1SG15EC060	MOHAMMED SHAHID
4.	1SG15EC088	RANJAN S
5.	1SG16EC001	ABHAY SINGH
6.	1SG16EC002	AISHWARYA G
7.	1SG16EC003	AJAY KUMAR S
8.	1SG16EC004	AJAY P S
9.	1SG16EC005	ALOK KUMAR
10.	1SG16EC006	ANANYA H R
11.	1SG16EC007	ANKITHA C S
12.	1SG16EC008	ANUSHA R
13.	1SG16EC009	ANUSHA SHETTY
14.	1SG16EC010	ARUNISH KUMAR
15.	1SG16EC012	ASHWINI S
16.	1SG16EC013	ASWINI D
17.	1SG16EC014	BHANU RAJ
18.	1SG16EC015	BHOOMIKA N
19.	1SG16EC017	BINDU B S
20.	1SG16EC018	BUMIKA.N
21.	1SG16EC019	CHANDANA V
22.	1SG16EC020	CHILUKURI MADHU VAMSI KRISHNA
23.	1SG16EC022	DEEPAK B S
24.	1SG16EC023	DEEPIKA V
25.	1SG16EC024	DEEPTHI M
26.	1SG16EC025	DIKSHITHA R
27.	1SG16EC026	DIMPLE BHATT
28.	1SG16EC027	DISHANTH R
29.	1SG16EC029	DIVYASHREE L
30.	1SG16EC030	G VIGNESH
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49.	1SG16EC051	LIKITHA MS
50.	1SG16EC052	MADEPPA
51.	1SG16EC053	MADHUCHANDRA D
52.	1SG16EC054	MADHUKESH N M
53.	1SG16EC055	MADHURA MADHUKAR HEGDE
54.	1SG16EC056	MOHAMMAD ANIS
55.	1SG16EC057	NA NITHYA SHREE
56.	1SG16EC059	NAVEED BAIG
57.	1SG16EC060	NAVEEN T
58.	1SG16EC062	NAYANA T R
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60.	1SG16EC125	YASHAVANTH J
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63.	1SG16EC407	BHARATHI V
64.	1SG16EC414	PAVAN RAJ
65.	1SG16EC419	RAHUL SINGH
66.	1SG16EC422	SAMITHA M
67.	1SG16EC424	SHARATH P
68.	1SG16EC427	STEVEN MENEGES
69.	1SG16EC433	VINAY R
70.	1SG17EC400	AKSHATHA O H
71.	1SG17EC401	ANVITHA S M
72.	1SG17EC407	HARSHINI P
73.	1SG17EC411	LOKESH KUMAR S
74.	1SG17EC413	MAMATHASHREE V

CLASS TEACHER

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Sapthagiri College of Engineering
Department of Electronics and Communication Engineering
Students Name List

Semester: 6th 'B' **Academic Year: 2018–19**

Sl. No	USN	Name of the student
1.	1SG15EC050	KOWSALYA S
2.	1SG15EC088	RANJITH GOWDA B
3.	1SG15EC092	SANDHYA V
4.	1SG15EC095	SANJAY KUMAR B N
5.	1SG15EC100	SHASHIKANT KUMAR
6.	1SG15EC111	USHA KIRAN S
7.	1SG15EC117	MANU N M
8.	1SG15EC118	ASHWIN JAYAN
9.	1SG15EC124	SHASHANK B S
10.	1SG16EC063	NESAR GAONKAR
11.	1SG16EC065	NIKHIL S BHARADWAJ
12.	1SG16EC066	NIKITHA G
13.	1SG16EC068	NIVEDITA MALIPATIL
14.	1SG16EC070	PAVITHRA R
15.	1SG16EC071	POOJA BASAVARAJ MORKI
16.	1SG16EC072	PRAHALAD Y R
17.	1SG16EC073	PRAMILA K S
18.	1SG16EC074	PRATEEK M K
19.	1SG16EC075	PRAVESH THAKUR
20.	1SG16EC076	PRIYA SHARMA
21.	1SG16EC077	PRIYANKA R
22.	1SG16EC078	PUNIT RANJAN VERMA
23.	1SG16EC080	RAHUL J
24.	1SG16EC081	RAIGOND VIJAYLAKSHMI P
25.	1SG16EC082	RAKESH N
26.	1SG16EC084	RAKSHITH B
27.	1SG16EC085	RAKSHITHA G
28.	1SG16EC088	RIMA
29.	1SG16EC089	ROHINI S
30.	1SG16EC090	ROHITH N
31.	1SG16EC091	ROOPASHREE V
32.	1SG16EC093	SADIYA ANJUM
33.	1SG16EC094	SAI MANGALA M V
34.	1SG16EC095	SAMIR GARAG
35.	1SG16EC096	SANGEETHA V
36.	1SG16EC097	SANJANA GOWDA R H
37.	1SG16EC098	SHARATH GOWDA R N
38.	1SG16EC099	SHOBHA M R
39.	1SG16EC100	SHRUTI C TIGANIBIDARI
40.	1SG16EC101	SHUBHAM JAISWAL
41.	1SG16EC102	SHUBHAM KHOSLA
42.	1SG16EC103	SHUBHAM SINGH
43.	1SG16EC104	SINDHU C
44.	1SG16EC105	SIRISHA C K
45.	1SG16EC106	SNEHA SUNIL VAIDYA
46.	1SG16EC107	SNEHIL SARKAR
47.	1SG16EC109	SOUMYA GURURAJ
48.	1SG16EC111	SPOORTHY G
49.	1SG16EC112	SREEKEERTHI S
50.	1SG16EC113	SRINIVAS V
51.	1SG16EC114	SUFIYAN ASHRAF
52.	1SG16EC115	SUHAS B M
53.	1SG16EC118	USHA Y G
54.	1SG16EC119	VASANTHA M
55.	1SG16EC120	VINAY R
56.	1SG16EC122	YASHODHARE K
57.	1SG16EC123	ZENKAR R
58.	1SG16EC124	SRINIVAS PRASAD V
59.	1SG16EC126	VARNA SHETTY
60.	1SG16EC129	MAHESH K
61.	1SG16EC130	NITHIN G
62.	1SG16EC131	SANTHOSHGAGAN T
63.	1SG17EC408	HEMANTH KUMAR
64.	1SG17EC409	HITESH K
65.	1SG17EC412	MAHESH N
66.	1SG17EC414	N YASHASWINI SHREE
67.	1SG17EC418	PUSHPALATHA P H
68.	1SG17EC419	RACHANA M
69.	1SG17EC420	REKHA T B
70.	1SG17EC422	SANTHOSH GOWDA B R

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Sapthagiri College of Engineering

Department of Electronics and Communication Engineering

Students Batch List

Semester: 6th 'A'

Academic Year: 2018–19

A1		
No	USN	Name of the student
1.	1SG16EC001	ABHAY SINGH
2.	1SG16EC002	AISHWARYA G
3.	1SG16EC003	AJAY KUMAR.S
4.	1SG16EC004	AJAY P S
5.	1SG16EC005	ALOK KUMAR
6.	1SG16EC006	ANANYA H R
7.	1SG16EC007	ANKITHA C S
8.	1SG16EC008	ANUSHA R
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22.	1SG16EC025	DIKSHITHA R
23.	1SG16EC026	DIMPLE BHATT
24.	1SG16EC400	ANUSHA R
25.	1SG16EC407	BHARATHI V

Class Teacher

A2		
No	USN	Name of the student
1.	1SG16EC027	DISHANTH R
2.	1SG16EC029	DIVYASHREE L
3.	1SG16EC030	G VIGNESH
4.	1SG16EC031	GARIMA SINGH
5.	1SG16EC033	HARSHA S
6.	1SG16EC034	HARSHITHA B M
7.	1SG16EC035	HARSHITHA K
8.	1SG16EC036	HEMANTH T B
9.	1SG16EC037	JAYANTH S
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15.	1SG16EC043	KISHORE KUMAR
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22.	1SG16EC051	LIKITHA MS
23.	1SG16EC052	MADEPPA
24.	1SG16EC053	MADHUCHANDRA D
25.	1SG16EC054	MADHUKESH N M

A3		
No	USN	Name of the student
1.	1SG16EC055	MADHURA MADHUKAR HEGDE
2.	1SG16EC056	MOHAMMAD ANIS
3.	1SG16EC057	NA NITHYA SHREE
4.	1SG16EC059	NAVEED BAIG
5.	1SG16EC060	NAVEEN T
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22.	1SG16EC424	SHARATH P
23.	1SG16EC427	STEVEN MENEGES
24.	1SG16EC433	VINAY R

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HOD,ECE

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DEPT. of ECE

Subject: **ARM Microcontroller and Embedded System** Sub. Code: **15EC62**

Sem / Sec : **VI A & B**

Assignment – 1

1. Give the 5 characteristics of ARM Cortex M3.
2. With neat block diagram explain the various units of ARM Cortex M3.
3. Explain the Register set of ARM Cortex M3 in detail with neat Diagram
4. Explain the operating modes of Cortex M3 with the timing diagram to switch the operating modes with the use of CONTROL register.
5. Explain the memory map and stack operation of Cortex M3.
6. Explain the reset sequence and debugging support of ARM Cortex M3 Microcontroller.
7. Explain the Interrupts and exceptions of Cortex M3 with the use of 3 Interrupt control registers.
8. Give the applications of ARM Cortex M3.

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SAPTHAGIRI COLLEGE OF ENGINEERING

DEPT. of ECE

Subject: **ARM Microcontroller and Embedded System** Sub. Code: **15EC62**

Sem / Sec : **VI A & B**

Assignment – 2

1. Explain the components of a typical embedded system in detail.
2. Explain the role of different types of Read only memories used embedded system design.
3. Explain in detail the SPI & I²Ccommunication interface with sequence of operation for communicating with a slave device
4. Explain the role of reset circuit and watch dog timer in embedded system
5. Write an ALP to find the sum of first 10 integer numbers 1+2+3…….+10.

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DEPT. of ECE

Subject: **ARM Microcontroller and Embedded System** Sub. Code: **15EC62**

Sem / Sec : **VI A & B**

Assignment – 3

1. With FSM model, explain the design and operation of automatic seat belt warning system.
2. Explain the High level language based embedded firmware development.
3. What is preemptive scheduling? Three processeswith process ID's P1,P2,P3 with estimated completion time 10,5,7 ms and priorities 1, 3, 2 (0 – Highest priority, 3 – Lowest priority) respectively enters the ready queue together. A new process P4 with estimated completion time 6ms and priority0 enters the ready queue after 5msof start of execution of P1. Calculate the average waiting time and turnaround time.
4. Explain the transition of process with state transition diagram.
5. Explain the different issues of H/W S/W co-design in embedded system design.

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USN	1	S	G							

SAPTHAGIRI COLLEGE OF ENGINEERING – Bangalore 560057
Department of Electronics and Communication
Internal Assessment –I

Subject: ARM Microcontroller and Embedded System **Sub Code: 15EC62**
Semester/Section: VI / A & B **Max Marks: 30**
Duration: 1.5 hours **Date: 11.03.19**
Answer any two full questions, choosing one from each module

Question No.	Questions	Marks	BTL	CO's
	Module-1			
1 a.	With neat diagram explain the architecture of Cortex M3	08	L2	CO1
1b.	Explain in detail the stack operations of Cortex M3.	07	L2	CO1
	(or)			
2 a.	Explain the functions of R0 to R15 registers and the three special function registers of Cortex M3	08	L2	CO1
2b.	Explain in detail the nested vector interrupt controller and reset sequence of cortexM3	07	L2	CO1
	Module – 2			
3a.	Explain the load and store operations supported by cortex M3.	08	L2	CO1
3b.	Explain in detail the shift and rotate instructions of Cortex M3	07	L2	CO1
	(or)			
4a.	Give the output after executing the following instructions Assume R0=0x00007E8F R1 = 0x00000007 (i)ADD R2,R1,R0 (ii) RSB R2, R1,R0 (iii) BIC R2,R1,R0 (iv) MUL R2,R1,R0	08	L3	CO1
4b.	Explain all 32bit Multiply instructions supported by cortex m3	03	L2	CO1
4c.	Explain the instructions of cortex M3 for moving immediate data to registers	04	L2	CO1

CO1: Students will be able to describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.

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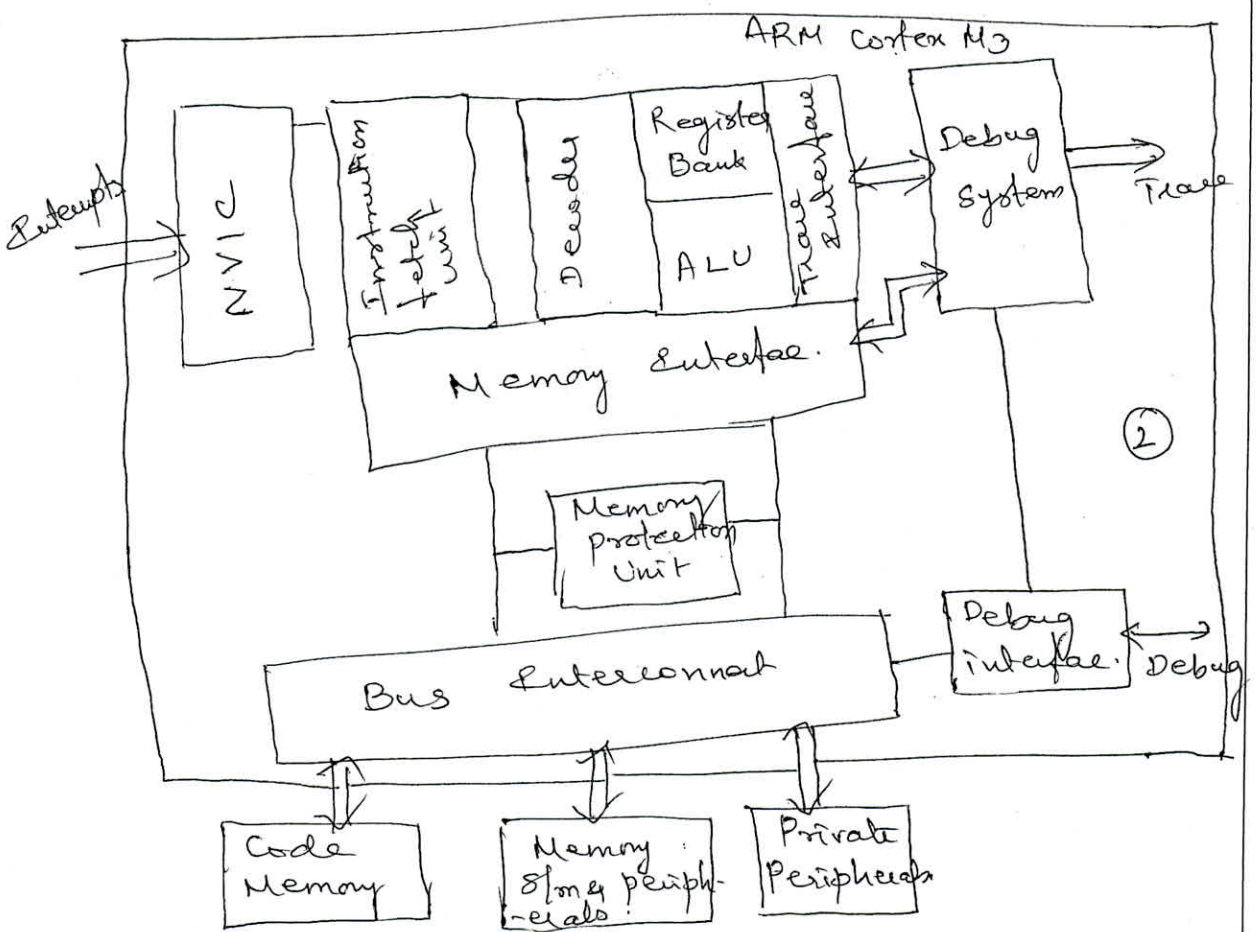
SAPTHAGIRI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHEME & SOLUTIONS

Subject /Code : ARM Microcontrollers & Embedded s/m
Duration / Date : 1.5hrs / 11.03.19
Staff Name : P. Agalya
Sem & section : VI A & B
Max. Marks : 30
Signature :

INTERNAL ASSESSMENT TEST- I

Question No.	SOLUTIONS	Marks allocated
1a)	Architecture of Cortex-M3	



(2)

Explanation

16, 32 bit Registers, 3 special purpose registers, NVIC, ALU, Register bank, Instruction Decoder, Debug system, Memory map (6)

(8)

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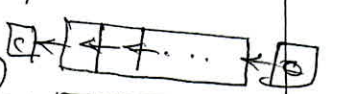
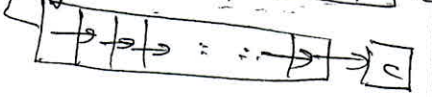
Qs No	Solutions	Marks Allocated
2b)	NVIC * Nested Interrupt support * Vectored " " * Dynamic priority changes support * Reduction of interrupt latency * Interrupt Masking	(7)
	Module - 2	
3a	load operation → LDRB, LDRH, LDR, LDRD. } loads byte, half word, word & double word from Memory ⇒ Registers. (2) LDMIA, LDMDB, — (1) pre indexing & post indexing — (1)	(8)
	store operation → STRB, STRH, STR, STRD } stores the data from Reg to Memory (2) STMIA, STMDB — (1) pre indexing & post indexing — (1)	
3b)	shift & Rotate instructions of Cortex-M3. logical → left shift (LSL)  → Right shift (LSR)  Arithmet Right shift (ASR) 	

USN	1	S	G							

SAPTHAGIRI COLLEGE OF ENGINEERING – Bangalore 560057
Department of Electronics and Communication
Internal Assessment –II

Subject: ARM Microcontroller and Embeddeded System **Sub Code: 15EC62**

Semester/Section: VI / A & B **Max Marks: 30**

Duration: 1.5 hours **Date: 15.04.19**

Note: Answer any two full questions, choosing one from each module

Question No.	Questions	Marks	RBTL	CO's
	Module-1			
1 a.	Write and explain the memory map of cortex M3 with its default attributes and access levels	7	L1,L2	CO2
1b.	Explain the following instructions with suitable example. (i)BFC (ii) SXTH (iii) UBFX (iv) BFI	8	L1	CO2
2 a.	Briefly explain the bit band operation support of Cortex M3	5	L2	CO2
2b.	Write an ALP to find the sum of first 10 integer numbers 1+2+3…+10	5	L1	CO2
2c.	Write a C language program to toggle an LED with a small delay in Cortex M3	5	L1	CO2
	Module - 2			
3a.	Differentiate between General Computing Systems and Embedded Systems.	5	L1	CO3
3b.	Define an Embedded system and explain the classifications of Embedded system.	5	L2	CO3
3c.	Mention the application areas and purpose of embedded system with examples	5	L1	CO3
4a.	With a neat diagram explain the components of typical Embedded Systems in detail	8	L2	CO3
4b.	Write short notes on (i) Little Endian and Big Endian architecture (ii) RISC and CISC architectures	7	L2	CO3

CO2	To describe the memory map of cortex m3 and apply the knowledge gained for Programming ARM Cortex M3 for different applications.
CO3	To apply the knowledge in selecting basic hardware components in the design of embedded system based on the characteristics and attributes of an embedded system.

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SAPTHAGIRI COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHEME & SOLUTIONS

Subject /Code : ARM Microcontroller & Es / 15EC62
Duration / Date : 1.5 hrs.
Staff Name : P. Agalya

Sem & section : VI A & B
Max. Marks : 30
Signature :

INTERNAL ASSESSMENT TEST- II

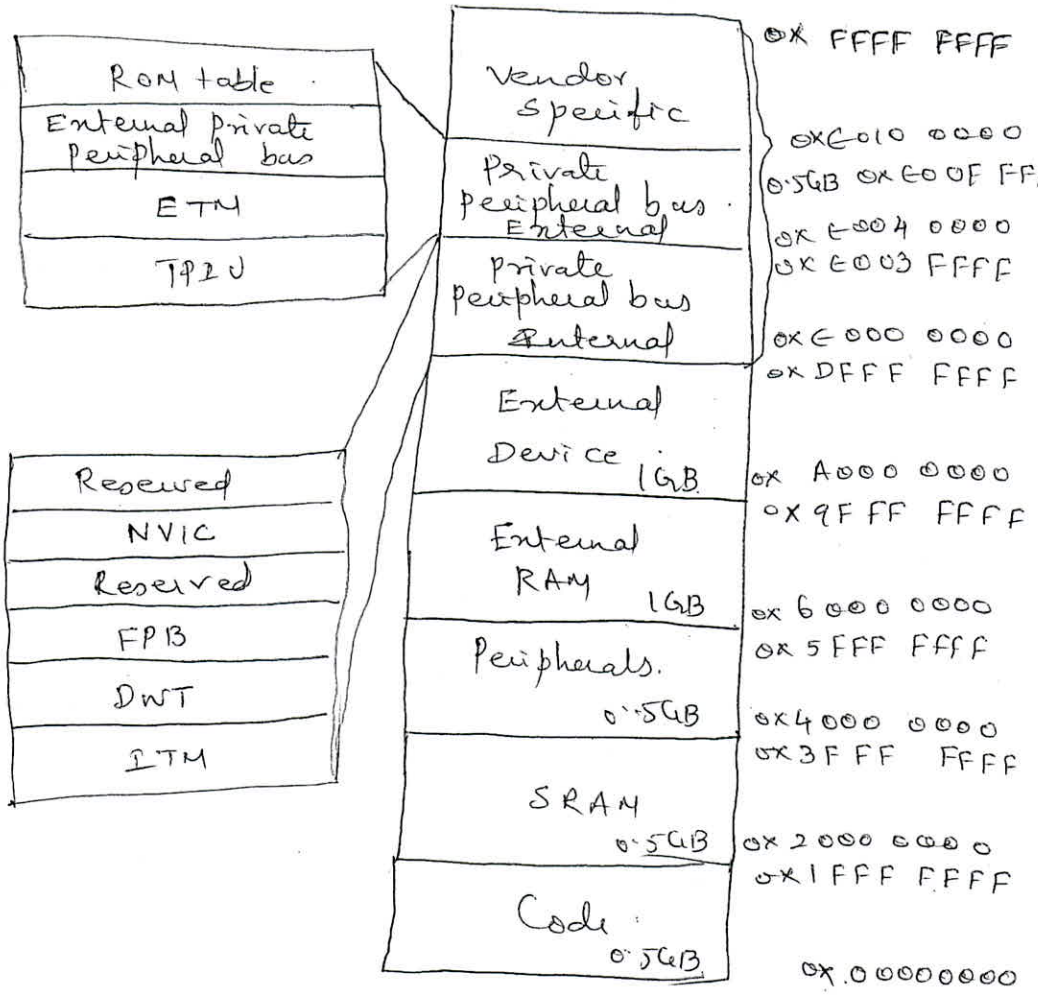
Question No.	SOLUTIONS	Marks allocated
1a)		7
1b)	BFc → Bit field clear → clears the bits in any position of a reg. BFc.W <Rd>, <#lsb>, <#width>	

Diagram – 2 Explanation – 5

Access attributes – 1 Access levels – 1

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Qs No	Solutions	Marks Allocated

```
Start :
        MOV r0, #10
        MOV r1, # 0
Loop :  ADD r1, r0
        SUBS r0, #1
        BNE Loop
Deadloop : B Deadloop
        END.
```

5

2c) C program to blink an LED

```
#define LED *(volatile unsigned int *)
                (0xDFFF000C))
int main (void)
volatile int i;
while (1) { LED = 0x00;
    for (i = 0; i < 1000; i++)
    LED = 0x01;
    for (i = 0; i < 1000; i++)
    } return 0;
    }
```

3a)

General computing s/m	Embedded s/m
(i) Combination of generic h/w & general purposes	(i) Special h/w + embedded OS
(ii) General purpose OS	(ii) May or may not contain OS
(iii) Applications are user alterable.	(iii) Non alterable by user
(iv) Performance is the key factor	(iv) Apln. specific requirements are key factors
(v) Not critical response time	(v) Critical response time.

5

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SAPTHAGIRI COLLEGE OF ENGINEERING – Bangalore 560057
Department of Electronics and Communication
Internal Assessment –III

Subject: ARM Microcontroller and Embeddeded System **Sub Code: 15EC62**

Se mester/Section: VI / A & B **Max Marks: 30**

Duration: 1.5 hours **Date: 16.05.19**

Note: Answer any two full questions, choosing one from each module

Question No.	Questions	Marks	BLT	CO's
	Module-4			
1 a.	Mention and explain the operational quality attributes of an embedded systems	08	L1,L2	CO4
1b.	Mention and explain the different characteristics of an embedded system.	07	L1,L2	CO4
2 a.	With FSM model explain the design of Seat belt warning system.	08	L2	CO4
2b.	With diagram explain the assembly language based embedded firmware design with advantages and drawbacks.	07	L2	CO4
	Module – 5			
3a.	Define Process & Threads. Describe the various states of a process its state transitions with a neat diagram.	08	L2	CO5
3b.	Describe preemptive SJF scheduling. Determine average turn around time and average waiting time, if processes P1 P2 and P3 with estimated completion time of 10, 5, 7 milliseconds enter ready queue together and later P4 with a completion time of 2 msec enters ready queue after 2 msec.	07	L3	CO5
4a.	Explain following task communication tools (i) Pipe & (ii) Memory Mapped Object.	08	L1	CO5
4b.	Explain the task synchronisation issues (i) Racing (ii) deadlock	07	L2	CO5

CO4:Students are able to develop an embedded system using the hardware /software co-design and firmware design approaches.

CO5: Students are able to explain the need of real time operating system for embedded system applications.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHEME & SOLUTIONS

Subject /Code : 15EC62
Duration / Date : 1.5 hrs
Staff Name : P. Agalya

Sem & section : 6 A & B
Max. Marks : 30
Signature :

INTERNAL ASSESSMENT TEST- 3

Question No.	SOLUTIONS	Marks allocated
1 a)	Operational Quality attributes. Response – Measure of quickness of system. ⇒ how fast the s/m tracks the i/p variables. Throughput – Deals with the efficiency of s/m. → rate of production. Reliability – % of relying on the proper functioning of the s/m. MTTR & MTBF used in defining s/m reliability. Maintainability – support & maintanance to the end user. scheduled & periodic maintanance. security – Confidentiality, availability & integrity are three major measures of security. Safety – possible damage that can happen to the OS & environment.	(8)
b)	Characteristics of an Embedded s/m. (i) Application & domain specific (ii) Real time & Reative. (iii) operates in harsh environment. & explanation (iv) Distributed (v) Small size & weight (vi) Power concerns.	(7)

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Qs No	Solutions	Marks Allocated

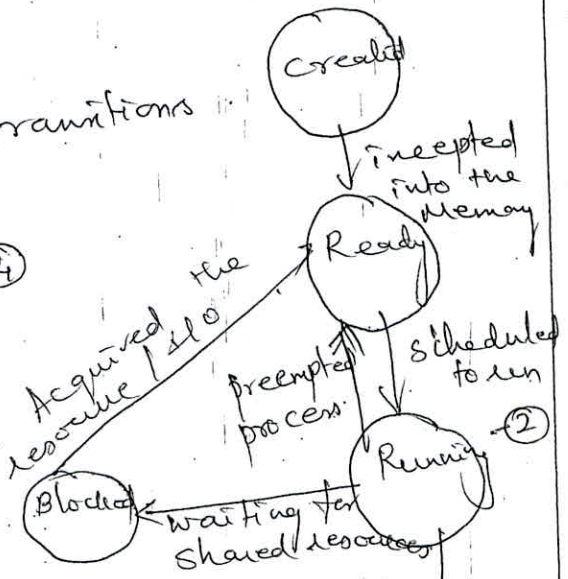
Module - 5

3a) Process : A small program (or) part of a program
→ an instance of a program in execution
→ It inherits all the features of a physical processor → virtual processor " — (1)
→ requires CPU, memory for storing the code & I/O devices.

Thread → It is a single sequential flow of control execution within a process
It is also known as lightweight process — (1)

8

process states & transitions



explanation — (4)

3b) preemptive SJF scheduling

shortest job is scheduled first. If a new job with less execution time than the remaining execution time of current running process, then the newly entered process is put to run state.

P_2	P_4	P_2	P_3	P_1
0	2	4	7	14	24

(1)

Waiting time
$P_1 = 14$ $P_3 = 7$ Average = $\frac{23}{4}$ = 5.75ms.
$P_2 = 2$ $P_4 = 0$
(3)

Turn around time
$P_1 = 24$ $P_3 = 14$
$P_2 = 7$ $P_4 = 2$
Average = 11.75ms.
(3)

7

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Sapthagiri College of Engineering
Department of Electronics and Communication Engineering
Invigilator's Diary

Sem: 6th ECE – A
Sub: ACAES / MP

Academic Year: 2018–19
Sub Code: 15EC62
10EC62

Sl.No.	USN	Name of the Student	I IA	II IA	III IA
			Date 11.3.19	Date 15.4.19	Date 16/05/19
			Room No: 307	Room No: 307	Room No:
1.	1SG15EC017	ASHWIN V			
2.	1SG15EC056	MANJUNATHA NAIK N			
3.	1SG15EC060	MOHAMMED SHAHID			
4.	1SG15EC088	RANJAN S			
5.	1SG16EC001	ABHAY SINGH			
6.	1SG16EC002	AISHWARYA G			
7.	1SG16EC003	AJAY KUMAR S			
8.	1SG16EC004	AJAY P S			
9.	1SG16EC005	ALOK KUMAR			
10.	1SG16EC006	ANANYA H R			
11.	1SG16EC007	ANKITHA C S			
12.	1SG16EC008	ANUSHA R			
13.	1SG16EC009	ANUSHA SHETTY			
14.	1SG16EC010	ARUNISH KUMAR			
15.	1SG16EC012	ASHWINI S			
16.	1SG16EC013	ASWINI D			
17.	1SG16EC014	BHANU RAJ			
18.	1SG16EC015	BHOOMIKA N			
19.	1SG16EC017	BINDU B S			
20.	1SG16EC018	BUMIKA.N			
21.	1SG16EC019	CHANDANA V			
22.	1SG16EC020	CHILUKURI MADHU VAMSI KRISHNA			
23.	1SG16EC022	DEEPAK B S			
24.	1SG16EC023	DEEPIKA V			
25.	1SG16EC024	DEEPTHI M			
No. of absentees			01	Nil	08
Name & signature of Faculty			Padmavathi C	VANI. A	Vinay H.C

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Invigilator's Diary

Sem: 6th ECE – A
Sub: ACAES / MP

Academic Year: 2018–19
Sub Code: 15EC62
10EC62

Sl.No.	USN	Name of the Student	I IA	II IA	III IA
			Date 11.3.19	Date 15.4.19	Date 16.5.19
			Room No: 308	Room No: 308	Room No: 308
1.	1SG16EC025	DIKSHITHA R	Dikshitha.R	Dikshitha.R	Dikshitha.R.
2.	1SG16EC026	DIMPLE BHATT	Dimple	Dimple	←ABSENT→
3.	1SG16EC027	DISHANTH R	Dishanth.R	Dishanth.R	Dishanth.R
4.	1SG16EC029	DIVYASHREE L	Deepal	Deepal	Deepal
5.	1SG16EC030	G VIGNESH	Dignal	Dignal	Dignal
6.	1SG16EC031	GARIMA SINGH	Garima	Garima	←ABSENT→
7.	1SG16EC033	HARSHA S	Aaishas	Aaishas	Aaishas
8.	1SG16EC034	HARSHITHA B M	Harshitha.B.M	Harshitha.B.M	Harshitha.B.M
9.	1SG16EC035	HARSHITHA K	H Sho.K	H Sho.K	H Sho.K
10.	1SG16EC036	HEMANTH T B			
11.	1SG16EC037	JAYANTH S	Jayanth.S	Jayanth.S	Jayanth.S
12.	1SG16EC038	KARTIK PRANESH KULKARNI	Kp.kulkarni		←ABSENT→
13.	1SG16EC039	KAVYA M	Kavya.M.	Kavya M.	Kavya M.
14.	1SG16EC040	KAVYA R	Kavya.R	Kavya.R	←ABSENT→
15.	1SG16EC041	KESHAV KUMAR BHANDARI	←ABSENT→	Keshav	Keshav
16.	1SG16EC042	KIRAN B N	Kiran.B.N.	Kiran.B.N.	Kiran.B.N.
17.	1SG16EC043	KISHORE KUMAR	Kishor.S.R	← AB →	Kishor.S.R
18.	1SG16EC044	KRITHIKA L	Krithika	Krithika	Krithika
19.	1SG16EC045	KUMARI PARUL	Parul	Parul	Parul
20.	1SG16EC047	LAVANYA K V	Lavanya.k	Lavanya.k	Lavanya
21.	1SG16EC048	LAVANYA P	Lavanya.P	Lavanya.P	Lavanya.P
22.	1SG16EC049	LEKHANA B S	Lekhana.B.S	Lekhana.B.S	Lekhana.B.S
23.	1SG16EC050	LIKHITHA B S	Likitha.B.S	Likitha.B.S	Likitha.B.S
24.	1SG16EC051	LIKITHA MS	Likitha.MS	← AB →	Likitha.MS
25.	1SG16EC052	MADEPPA	Madeppa.C	Madeppa.C.	MADEPPA.C.
Name & signature of Faculty			Thippeswamy.E	SPILPA V.	VANI.A
				Shilpa V.	

15/4/19.

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Department of Electronics and Communication Engineering
Invigilator's Diary

Sem: 6th ECE - A
Sub: ACAES / MP

Academic Year: 2018-19
Sub Code: 15EC62
10EC62

Sl.No.	USN	Name of the Student	I IA	II IA	III IA
			Date 11.3.19	Date 15.4.19	Date 16/05/19
			Room No: 309	Room No: 309	Room No: 307
1.	1SG16EC053	MADHUCHANDRA D	Madhu.D	Madhu.D	Madhu.D
2.	1SG16EC054	MADHUKESH N M	Madhukesh.N.M	Madhukesh.N.M	Madhukesh.N.M
3.	1SG16EC055	MADHURA MADHUKAR HEGDE	Madhura	Madhura	Madhura
4.	1SG16EC056	MOHAMMAD ANIS	Anis	Anis	Absent
5.	1SG16EC057	NA NITHYA SHREE	N.A. Nithyashree	N.A. Nithyashree	Absent
6.	1SG16EC059	NAVEED BAIG	Naveedbaig	Naveedbaig	Naveedbaig
7.	1SG16EC060	NAVEEN T	Naveen	Naveen	Naveen
8.	1SG16EC062	NAYANA T R	Nayana	Nayana	Nayana
9.	1SG16EC064	NIDHI S	Nidhi	Nidhi	Nidhi
10.	1SG16EC125	YASHAVANTH J	M.P	Absent	J M.P
11.	1SG16EC127	KUSHAL M P		Absent	
12.	1SG16EC400	ANUSHA R	Anusha.R	Anusha.R	Anusha.R
13.	1SG16EC407	BHARATHI V	Bharathi.V	Bharathi.V	Bharathi.V
14.	1SG16EC414	PAVAN RAJ	Pavan Raj.K	Pavan Raj.K	Pavan Raj.K
15.	1SG16EC419	RAHUL SINGH	Rahul	Rahul	Rahul
16.	1SG16EC422	SAMITHA M	S Samitha.M	S Samitha.M	S Samitha.M
17.	1SG16EC424	SHARATH P	Sharath.P	Sharath.P	Sharath.P
18.	1SG16EC427	STEVEN MENEGES	Steven	Steven	Steven
19.	1SG16EC433	VINAY R	Vinay.R	Vinay.R	Vinay.R
20.	1SG17EC400	AKSHATHA O H	Akshatha.O.H	Akshatha.O.H	Akshatha.O.H
21.	1SG17EC401	ANVITHA S M	Anvitha.S.M	Anvitha.S.M	Anvitha.S.M
22.	1SG17EC407	HARSHINI P	Harshini.P	Absent	Harshini.P
23.	1SG17EC411	LOKESH KUMAR S	Lokesh Kumar.S	Lokesh Kumar.S	Lokesh Kumar.S
24.	1SG17EC413	MAMATHASHREE V	Mamathashree	Mamathashree	Mamathashree
No. of absentees			NIL	03	02
Name & signature of Faculty			Thimmaraja Y.H	Thimmaraja Y.H	Thimmaraja Y.H

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Sem: 6th ECE – B
Sub: ACAES / MP

Academic Year: 2018–19
Sub Code: 15EC62
10EC62

Sl.No.	USN	Name of the Student	I IA	II IA	III IA
			Date 11-3-19	Date 15-4-19	Date 16/5/19
			Room No: ~~30~~ 311	Room No: 311	Room No: 311
1.	1SG15EC050	KOWSALYA S	Kowsalya	Kowsalya	A
2.	1SG15EC088	RANJITH GOWDA B	Ranjith	Ranjith	A
3.	1SG15EC092	SANDHYA V	Sandhya	Sandhya	A
4.	1SG15EC095	SANJAY KUMAR B N	Sanjay	Sanjay	A
5.	1SG15EC100	SHASHIKANT KUMAR	– ABSENT –		A
6.	1SG15EC111	USHA KIRAN S	Usha	Usha	A
7.	1SG15EC117	MANU N M	Manu	(A)	A
8.	1SG15EC118	ASHWIN JAYAN	Ashwin	Ashwin	A
9.	1SG15EC124	SHASHANK B S	Shashank	(A)	A
10.	1SG16EC063	NESAR GAONKAR	Nesar	(A)	A
11.	1SG16EC065	NIKHIL S BHARADWAJ	Nikhil	Nikhil	A
12.	1SG16EC066	NIKITHA G	– ABSENT –	G. Nikitha	G. Nikitha
13.	1SG16EC068	NIVEDITA MALIPATIL	Nivedita	Nivedita	A
14.	1SG16EC070	PAVITHRA R	Pavithra. R	Pavithra. R	A
15.	1SG16EC071	POOJA BASAVARAJ MORKI	Pooja	Pooja	A
16.	1SG16EC072	PRAHALAD Y R	Prahalad. Y. R	Prahalad. Y. R.	Prahalad. Y. R.
17.	1SG16EC073	PRAMILA K S	Pramila K S	Pramila K S	A
18.	1SG16EC074	PRATEEK M K	Prateek. M. K	Prateek. M. K	Prateek. M. K
19.	1SG16EC075	PRAVESH THAKUR	Pthakur	(A)	Pthakur
20.	1SG16EC076	PRIYA SHARMA	– ABSENT –	Priya	Priya
21.	1SG16EC077	PRIYANKA R	Priyanka	(A)	Priyanka
22.	1SG16EC078	PUNIT RANJAN VERMA	Punit	(A)	Punit
23.	1SG16EC080	RAHUL J	Rahul. J	Rahul. J	Rahul. J
24.	1SG16EC081	RAIGOND VIJAYLAKSHMI P	Rajgond	Rajgond	Rajgond
No. of absentees			03	05	07
Name & signature of Faculty			Vinay H.C	Suma V Shetty	Suma V Shetty

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Invigilator's Diary

Sem: 6th ECE - B
Sub: ACAES / MP

Academic Year: 2018-19
Sub Code: 15EC62 / 10EC62

Sl.No.	USN	Name of the Student	I IA	II IA	III IA
			Date 11.3.19	Date 15.4.19	Date 16.5.19
			Room No: 312	Room No: 312	Room No: 312
1.	1SG16EC082	RAKESH N			
2.	1SG16EC084	RAKSHITH B			
3.	1SG16EC085	RAKSHITHA G			
4.	1SG16EC088	RIMA			
5.	1SG16EC089	ROHINI S			
6.	1SG16EC090	ROHITH N			
7.	1SG16EC091	ROOPASHREE V			
8.	1SG16EC093	SADIYA ANJUM			
9.	1SG16EC094	SAI MANGALA M V			AB
10.	1SG16EC095	SAMIR GARAG			AB
11.	1SG16EC096	SANGEETHA V			
12.	1SG16EC097	SANJANA GOWDA R H		AB	
13.	1SG16EC098	SHARATH GOWDA R N			AB
14.	1SG16EC099	SHOBHA M R			
15.	1SG16EC100	SHRUTI C TIGANIBIDARI			
16.	1SG16EC101	SHUBHAM JAISWAL			AB
17.	1SG16EC102	SHUBHAM KHOSLA			
18.	1SG16EC103	SHUBHAM SINGH	ABSENT		
19.	1SG16EC104	SINDHU C	ABSENT		
20.	1SG16EC105	SIRISHA C K		AB	
21.	1SG16EC106	SNEHA SUNIL VAIDYA			
22.	1SG16EC107	SNEHIL SARKAR			
23.	1SG16EC109	SOUMYA GURURAJ		AB	
No. of absentees			02	03	04
Name & signature of Faculty					

21 | 20 | 20/20

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Department of Electronics and Communication Engineering
Invigilator's Diary

Sem: 6th ECE – B & Parallel course
Sub: ACAES / MP

Academic Year: 2018–19
Sub Code: 15EC62
10EC62

Sl.No.	USN	Name of the Student	I IA	II IA	III IA
			Date 11.3.19	Date 15.4.19	Date 16-5-19
			Room No: 313	Room No: 313	Room No:
1.	1SG16EC111	SPOORTHY G		AB	
2.	1SG16EC112	SREEKEERTHI S		AB	
3.	1SG16EC113	SRINIVAS V			
4.	1SG16EC114	SUFIYAN ASHRAF	Sufiyan Ashraf	Sufiyan Ashraf	Sufiyan Ashraf
5.	1SG16EC115	SUHAS B M	Suhas.B.M.	Suhas.B.M.	Suhas.B.M.
6.	1SG16EC118	USHA Y G	Usha.Y.G	Usha.Y.G	Usha.Y.G
7.	1SG16EC119	VASANTHA M	Vasantha.M	AB	Vasantha.M
8.	1SG16EC120	VINAY R	V. R	V. R	V. R
9.	1SG16EC122	YASHODHARE K		AB	
10.	1SG16EC123	ZENKAR R	Zenkar R.	Zenkar R.	
11.	1SG16EC124	SRINIVAS PRASAD V			AB
12.	1SG16EC126	VARNA SHETTY			
13.	1SG16EC129	MAHESH K	K. Mahesh.	K. Mahesh	K. Mahesh
14.	1SG16EC130	NITHIN G			
15.	1SG16EC131	SANTHOSHGAGAN T			
16.	1SG17EC408	HEMANTH KUMAR	Hemanth	Hemanth	Hemanth
17.	1SG17EC409	HITESH K	Hithush.K	Hithush.K	Hithush.K
18.	1SG17EC412	MAHESH N			
19.	1SG17EC414	N YASHASWINI SHREE	Yashu.	Yashu.	AB
20.	1SG17EC418	PUSHPALATHA P H			AB
21.	1SG17EC419	RACHANA M		Rachana.M	Rachana.M
22.	1SG17EC420	REKHA T B	AB	Rekha B.	Rekha B
23.	1SG17EC422	SANTHOSH GOWDA B R	AB		
24.	1SG13EC032 (PARALLEL COURSE)	BHAVANA JAIN	Santhosh Gowda. Bhavana H.N	Santhosh Gowda Bhavana H.N	Santhosh Gowda. Bhavana H.N.
No. of absentees			02	04	03
Name & signature of Faculty			Shobha H	NAMRATHA.V	NAMRATHA.V

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SAPTHAGIRI COLLEGE OF ENGINEERING
DEPARTMENT OF ECE
INTERNAL ASSESMENT TEST MARKS

Semester : 6th 'A'

Sl. No.	USN	Name of the student	15EC62					
			IA-1	IA-2	IA-3	A	AVG	A+AV
								20
1	1SG15EC017	ASHWIN V	10	16	27	5	12	17
2	1SG15EC056	MANJUNATHA NAIK N	5	10	22	5	8	13
3	1SG15EC060	MOHAMMED SHAHID	14	10	AB	5	7	12
4	1SG15EC088	RANJAN S	7	19	8	5	8	13
5	1SG16EC001	ABHAY SINGH	4	12	17	5	8	13
6	1SG16EC002	AISHWARYA G	20	13	23	5	11	16
7	1SG16EC003	AJAY KUMAR S	22	27	AB	5	13	18
8	1SG16EC004	AJAY P S	12	14	16	5	8	13
9	1SG16EC005	ALOK KUMAR	25	26	27	5	14	19
10	1SG16EC006	ANANYA H R	23	18	AB	5	11	16
11	1SG16EC007	ANKITHA C S	17	13	27	5	14	19
12	1SG16EC008	ANUSHA R	19	19	AB	5	10	15
13	1SG16EC009	ANUSHA SHETTY	10	10	21	5	8	13
14	1SG16EC010	ARUNISH KUMAR	ab	19	17	5	10	15
15	1SG16EC012	ASHWINI S	24	18	24	5	12	17
16	1SG16EC013	ASWINI D	25	21	29	5	15	20
17	1SG16EC014	BHANU RAJ	13	18	AB	5	8	13
18	1SG16EC015	BHOOMIKA N	10	12	13	5	7	12
19	1SG16EC017	BINDU B S	17	19	AB	5	10	15
20	1SG16EC018	BUMIKA.N	19	24	20	5	11	16
21	1SG16EC019	CHANDANA V	8	9	28	5	10	15
22	1SG16EC020	CHILUKURI MADHU VAMSI KRISHNA	24	23	AB	5	12	17
23	1SG16EC022	DEEPAK B S	14	20	AB	5	9	14
24	1SG16EC023	DEEPIKA V	25	28	AB	5	15	20
25	1SG16EC024	DEEPTHI M	13	27	29	5	15	20
26	1SG16EC025	DIKSHITHA R	14	15	21	5	10	15
27	1SG16EC026	DIMPLE BHATT	24	25	AB	5	13	18
28	1SG16EC027	DISHANTH R	18	20	26	5	12	17
29	1SG16EC029	DIVYASHREE L	19	27	27	5	14	19
30	1SG16EC030	G VIGNESH	9	14	26	5	10	15
31	1SG16EC031	GARIMA SINGH	20	17	AB	5	10	15
32	1SG16EC033	HARSHA S	15	15	25	5	11	16
33	1SG16EC034	HARSHITHA B M	20	19	21	5	11	16
34	1SG16EC035	HARSHITHA K	17	19	27	5	12	17
35	1SG16EC036	HEMANTH T B	13	21	22	5	11	16

36	1SG16EC037	JAYANTH S	16	20	26	5	12	17
37	1SG16EC038	KARTIK PRANESH KULKARNI	19	19	AB	5	10	15
38	1SG16EC039	KAVYA M	20	19	26	5	12	17
39	1SG16EC040	KAVYA R	19	21	AB	5	11	16
40	1SG16EC041	KESHAV KUMAR BHANDARI	ab	12	13	5	7	12
41	1SG16EC042	KIRAN B N	14	16	27	5	11	16
42	1SG16EC043	KISHORE KUMAR	18	ab	21	5	10	15
43	1SG16EC044	KRITHIKA L	11	14	15	5	8	13
44	1SG16EC045	KUMARI PARUL	13	18	22	5	10	15
45	1SG16EC047	LAVANYA K V	22	20	22	5	13	18
46	1SG16EC048	LAVANYA P	17	21	30	5	13	18
47	1SG16EC049	LEKHANA B S	13	17	20	5	10	15
48	1SG16EC050	LIKHITHA B S	17	17	20	5	10	15
49	1SG16EC051	LIKITHA MS	14	ab	27	5	11	16
50	1SG16EC052	MADEPPA	12	12	23	5	9	14
51	1SG16EC053	MADHUCHANDRA D	10	11	22	5	9	14
52	1SG16EC054	MADHUKESH N M	14	13	17	5	8	13
53	1SG16EC055	HEGDE	13	12	21	5	9	14
54	1SG16EC056	MOHAMMAD ANIS	12	18	AB	5	8	13
55	1SG16EC057	NA NITHYA SHREE	26	27	AB	5	14	19
56	1SG16EC059	NAVEED BAIG	10	13	26	5	10	15
57	1SG16EC060	NAVEEN T	9	19	18	5	10	15
58	1SG16EC062	NAYANA T R	14	25	24	5	13	18
59	1SG16EC064	NIDHI S	11	20	25	5	12	17
60	1SG16EC125	YASHAVANTH J	15	ab	14	5	8	13
61	1SG16EC127	KUSHAL M P	15	ab	14	5	8	13
62	1SG16EC400	ANUSHA R	8	15	11	5	7	12
63	1SG16EC407	BHARATHI V	11	10	11	5	7	12
64	1SG16EC414	PAVAN RAJ	9	15	20	5	9	14
65	1SG16EC419	RAHUL SINGH	6	14	10	5	7	12
66	1SG16EC422	SAMITHA M	18	19	16	5	10	15
67	1SG16EC424	SHARATH P	9	16	14	5	8	13
68	1SG16EC427	STEVEN MENEGES	19	19	19	5	10	15
69	1SG16EC433	VINAY R	7	18	26	5	11	16
70	1SG17EC400	AKSHATHA O H	6	12	24	5	9	14
71	1SG17EC401	ANVITHA S M	9	10	25	5	9	14
72	1SG17EC407	HARSHINI P	4	ab	8	5	7	12
73	1SG17EC411	LOKESH KUMAR S	7	12	15	5	7	12
74	1SG17EC413	MAMATHASHREE V	7	13	21	5	9	14

TOTAL NUMBER OF STUDENTS	**74**	**74**	**74**	**74**	**74**	**74**
NUMBER OF STUDENTS WITH <12	24	7	5	74	54	0
NUMBER OF STUDENTS WITH >=12	48	62	54	0	20	74
Number of Absentees	2	5	15	0	0	0

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SAPTHAGIRI COLLEGE OF ENGINEERING

DEPARTMENT OF ECE

INTERNAL ASSESMENT TEST MARKS

Semester : 6th 'B'

Sl. No.	USN	Name of the student	15EC62					
			IA-1	IA-2	IA-3	A	AVG	A+AV
								20
1	1SG15EC050	KOWSALYA S	12	21	AB	5	9	14
2	1SG15EC088	RANJITH GOWDA B	13	17	AB	5	8	13
3	1SG15EC092	SANDHYA V	14	20	AB	5	9	14
4	1SG15EC095	SANJAY KUMAR B N	8	18	AB	5	7	12
5	1SG15EC100	SHASHIKANT KUMAR	ab	13	12	5	7	12
6	1SG15EC111	USHA KIRAN S	11	19	AB	5	8	13
7	1SG15EC117	MANU N M	5	10	15	5	7	12
8	1SG15EC118	ASHWIN JAYAN	4	ab	21	5	7	12
9	1SG15EC124	SHASHANK B.S.	5	7	17	5	7	12
10	1SG16EC063	NESAR GAONKAR	17	ab	24	5	11	16
11	1SG16EC065	NIKHIL S BHARADWAJ	22	23	27	5	13	18
12	1SG16EC066	NIKITHA G	ab	20	27	5	12	17
13	1SG16EC068	NIVEDITA MALIPATIL	11	22	25	5	12	17
14	1SG16EC070	PAVITHRA R	26	24	AB	5	13	18
15	1SG16EC071	POOJA BASAVARAJ MORKI	14	26	22	5	12	17
16	1SG16EC072	PRAHALAD Y R	10	18	8	5	7	12
17	1SG16EC073	PRAMILA K S	25	26	AB	5	13	18
18	1SG16EC074	PRATEEK M K	24	17	26	5	13	18
19	1SG16EC075	PRAVESH THAKUR	16	ab	20	5	9	14
20	1SG16EC076	PRIYA SHARMA	ab	17	21	3	10	13
21	1SG16EC077	PRIYANKA R	11	ab	10	5	8	13
22	1SG16EC078	PUNIT RANJAN VERMA	11	ab	25	5	7	12
23	1SG16EC080	RAHUL J	17	13	25	5	11	16
24	1SG16EC081	RAIGOND VIJAYLAKSHMI P	15	13	24	5	11	16
25	1SG16EC082	RAKESH N	23	25	29	5	14	19
26	1SG16EC084	RAKSHITH B	14	16	16	5	8	13
27	1SG16EC085	RAKSHITHA G	11	23	28	5	13	18
28	1SG16EC088	RIMA	11	19	28	5	12	17
29	1SG16EC089	ROHINI S	12	15	22	5	10	15
30	1SG16EC090	ROHITH N	15	19	13	5	9	14
31	1SG16EC091	ROOPASHREE V	19	24	29	5	14	19
32	1SG16EC093	SADIYA ANJUM	22	27	AB	5	13	18
33	1SG16EC094	SAI MANGALA M V	19	28	AB	5	12	17
34	1SG16EC095	SAMIR GARAG	3	18	18	5	9	14
35	1SG16EC096	SANGEETHA V	16	ab	20	5	9	14
36	1SG16EC097	SANJANA GOWDA R H	17	19	AB	5	10	15
37	1SG16EC098	SHARATH GOWDA R N	14	18	20	5	10	15
38	1SG16EC099	SHOBHA M R	21	26	29	5	14	19
39	1SG16EC100	SHRUTI C TIGANIBIDARI	16	23	AB	5	10	15
40	1SG16EC101	SHUBHAM JAISWAL	13	21	25	5	12	17
41	1SG16EC102	SHUBHAM KHOSLA	ab	11	8	5	7	12
42	1SG16EC103	SHUBHAM SINGH	ab	12	16	5	7	12
43	1SG16EC104	SINDHU C	10	ab	25	5	9	14

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44	1SG16EC105	SIRISHA C K	6	16	20	5	9	14
45	1SG16EC106	SNEHA SUNIL VAIDYA	12	8	18	5	8	13
46	1SG16EC107	SNEHIL SARKAR	20	ab	23	5	11	16
47	1SG16EC109	SOUMYA GURURAJ	5	23	19	5	11	16
48	1SG16EC111	SPOORTHY G	13	ab	27	5	11	16
49	1SG16EC112	SREEKEERTHI S	26	ab	29	5	14	19
50	1SG16EC113	SRINIVAS V	19	18	22	5	11	16
51	1SG16EC114	SUFIYAN ASHRAF	9	11	16	5	7	12
52	1SG16EC115	SUHAS B M	29	18	28	5	15	20
53	1SG16EC118	USHA Y G	10	25	27	5	14	19
54	1SG16EC119	VASANTHA M	15	ab	27	5	11	16
55	1SG16EC120	VINAY R	9	18	20	5	10	15
56	1SG16EC122	YASHODHARE K	17	ab	23	5	11	16
57	1SG16EC123	ZENKAR R	13	17	26	5	11	16
58	1SG16EC124	SRINIVAS PRASAD V	14	24	AB	5	10	15
59	1SG16EC126	VARNA SHETTY	14	22	28	5	13	18
60	1SG16EC129	MAHESH K	16	8	15	5	12	17
61	1SG16EC130	NITHIN G	**13**	**8**	**19**	5	**9**	14
62	1SG16EC131	SANTHOSHGAGAN T	9	8	13	5	7	12
63	1SG17EC408	HEMANTH KUMAR	12	14	23	5	10	15
64	1SG17EC409	HITESH K	13	11	8	5	7	12
65	1SG17EC412	MAHESH N	13	10	7	5	7	12
66	1SG17EC414	N YASHASWINI SHREE	17	21	AB	5	10	15
67	1SG17EC418	PUSHPALATHA P H	14	21	AB	5	9	14
68	1SG17EC419	RACHANA M	ab	12	15	5	7	12
69	1SG17EC420	REKHA T B	ab	18	28	5	12	17
70	1SG17EC422	SANTHOSH GOWDA B R	8	18	15	5	9	14

TOTAL NUMBER OF STUDENTS	70	70	70	70	70	
NUMBER OF STUDENTS WITH <12	20	10	5	70	49	
NUMBER OF STUDENTS WITH >=12	43	48	51	0	21	
Number of Absentees	7	12	14	0	0	

NAME OF THE FACULTY

SIGNATURE OF FACULTY

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SAPTHAGIRI
COLLEGE OF ENGINEERING
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Individual Staff Appraisal

Staff Name:AGALYA P	Sub Code:15EC62	Sub Name:ARM Microcontroller & Embedded Systems
Section:~~2L~~ 6A	Department:ECE	Total Students given Feedback:56

Sl.No	Questions	Total Rating	Out of	Max Per(%)
1	Adequacy Of Learning Material Provided.	537	560.0	95.89
2	Audibility/Clarity of Lecture.	547	560.0	97.68
3	Availability Of the Faculty After the Class Hours.	552	560.0	98.57
4	Chalk-Talk/ICT Tools Usage.	550	560.0	98.21
5	Interaction with the students in the class.	542	560.0	96.79
6	Impartial assessment of Students.	552	560.0	98.57
7	Discipline & Control on the class.	547	560.0	97.68
8	Planning Of Effective Teaching.	552	560.0	98.57
9	Regular & Punctual to the Classes.	554	560.0	98.93
10	Syllabus Coverage as per the Lesson Plan.	546	560.0	97.50
	Total :	5479	5600	97.84

HOD Review:

Excellent, Keep it up

HOD SIGNATURE
Head of the Department
Electronics & Communication
Sapthagiri College of Engineering
Bangalore-560 057

Principal
Sapthagiri College of Engineering
Chikkasandra, Hesaraghatta Road,
Bangalore-560 057

SAPTHAGIRI
COLLEGE OF ENGINEERING
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Individual Staff Appraisal

Staff Name:AGALYA P	Sub Code:15EC62	Sub Name:ARM Microcontroller & Embedded Systems
Section:~~2L~~ 6B	Department:ECE	Total Students given Feedback:69

Sl.No	Questions	Total Rating	Out of Max	Per(%)
1	Adequacy Of Learning Material Provided.	668	690.0	96.81
2	Audibility/Clarity of Lecture.	664	690.0	96.23
3	Availability Of the Faculty After the Class Hours.	671	690.0	97.25
4	Chalk-Talk/ICT Tools Usage.	666	690.0	96.52
5	Interaction with the students in the class.	675	690.0	97.83
6	Impartial assessment of Students.	668	690.0	96.81
7	Discipline & Control on the class.	671	690.0	97.25
8	Planning Of Effective Teaching.	656	690.0	95.07
9	Regular & Punctual to the Classes.	672	690.0	97.39
10	Syllabus Coverage as per the Lesson Plan.	647	690.0	93.77
	Total :	6658	6900	96.49

HOD Review:

Excellent, keep it up

HOD SIGNATURE

Head of the Department
Electronics & Communication
Sapthagiri College of Engineering
Bangalore-560 057

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Bangalore-560 057

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Individual Staff Appraisal

Staff Name: AGALYA P Sub Code:ARM Microcontroller & Embedded Systems Sub Name:15EC62

Section:6A Department:ECE

Sl.No	Questions	Total Rating Points	Out of Max	Percentage(%)
1	Adequacy Of Learning Material Provided.	301	335.0	89.850746
2	Audibility Of Voice In The Class Room.	303	335.0	90.44776
3	Availability Of The Faculty After The Class Hours For Clearing The Doubts And For The Counseling Of Students.	306	335.0	91.343285
4	Effective Usage Of Black Board.	304	335.0	90.74627
5	Encouragement to Students for rising doubts/questions in the class.	304	335.0	90.74627
6	Impartial To All The Students.	311	335.0	92.83582
7	Maintaining Discipline & Control Over the Student	305	335.0	91.04478
8	Planning Of Lessons, Helping in Understanding the concepts with illustrative examples & effective explanation.	304	335.0	90.74627
9	Regularity & Punctuality In Engaging the Classes.	307	335.0	91.64179
10	Syllabus Coverage & depth of coverage.	298	335.0	88.95522
	Total:	3043	3350	90.83582

4/4/19

Head of the Department
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Bangalore-560 057

SAPTHAGIRI
COLLEGE OF ENGINEERING
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Individual Staff Appraisal

Staff Name: AGALYA P Sub Code:ARM Microcontroller & Embedded Systems Sub Name:15EC62

Section:6B Department:ECE

Sl.No	Questions	Total Rating Points	Out of Max	Percentage(%)
1	Adequacy Of Learning Material Provided.	186	205.0	90.73171
2	Audibility Of Voice In The Class Room.	182	205.0	88.78049
3	Availability Of The Faculty After The Class Hours For Clearing The Doubts And For The Counseling Of Students.	187	205.0	91.21951
4	Effective Usage Of Black Board.	190	205.0	92.68293
5	Encouragement to Students for rising doubts/questions in the class.	190	205.0	92.68293
6	Impartial To All The Students.	189	205.0	92.19512
7	Maintaining Discipline & Control Over the Student	185	205.0	90.2439
8	Planning Of Lessons, Helping in Understanding the concepts with illustrative examples & effective explanation.	184	205.0	89.756096
9	Regularity & Punctuality In Engaging the Classes.	189	205.0	92.19512
10	Syllabus Coverage & depth of coverage.	187	205.0	91.21951
	Total:	1869	2050	91.17073

4/4/15

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Visvesvaraya Technological University

SAPTHAGIRI COLLEGE OF ENGINEERING BENGALURU

Branch : EC Scheme : 2015 Semester : 6

Sl NO.	USN	15EC61	15EC62	15EC63	15EC64	15EC654	15EC663	15ECL67	15ECL68	STUDENT SIGNATURE
1	1SG15EC017	12	17	19	19	16	12	19	19	
2	1SG15EC050	15	14	16	15	17	13	19	18	
3	1SG15EC056	13	13	12	16	17	12	18	16	
4	1SG15EC060	12	12	12	12	13	10	16	15	
5	1SG15EC088	12	13	16	13	12	14	19	19	
6	1SG15EC089	15	13	17	13	16	12	19	18	
7	1SG15EC092	13	14	14	17	16	15	19	15	
8	1SG15EC095	13	12	14	13	17	14	18	16	
9	1SG15EC100	12	12	12	12	12	10	12	13	
10	1SG15EC111	13	13	15	16	16	13	19	16	
11	1SG15EC117	12	12	12	12	17	12	16	13	
12	1SG15EC118	10	12	12	13	14	10	17	15	
13	1SG15EC124	12	12	12	12	16	12	15	15	
14	1SG16EC001	13	13	12	13	18	12	15	14	
15	1SG16EC002	15	16	16	18	17	17	20	16	
16	1SG16EC003	19	18	20	20	20	20	19	19	
17	1SG16EC004	15	13	14	16	18	16	19	15	
18	1SG16EC005	17	19	17	20	20	20	19	18	
19	1SG16EC006	17	16	19	18	20	16	20	16	
20	1SG16EC007	18	19	19	18	19	20	20	17	
21	1SG16EC008	18	15	18	20	20	18	19	15	
22	1SG16EC009	12	13	15	13	13	14	19	14	
23	1SG16EC010	12	15	12	15	19	17	19	17	
24	1SG16EC012	17	17	18	19	20	18	20	17	
25	1SG16EC013	20	20	20	19	20	20	20	19	
26	1SG16EC014	12	13	12	17	16	13	18	15	
27	1SG16EC015	11	12	16	17	15	16	17	14	
28	1SG16EC017	18	15	17	19	20	19	18	16	
29	1SG16EC018	19	16	19	20	20	20	20	19	
30	1SG16EC019	14	15	16	13	14	13	17	17	
31	1SG16EC020	18	17	17	15	20	20	19	17	
32	1SG16EC022	12	14	18	18	20	13	19	15	
33	1SG16EC023	20	20	20	20	20	20	20	18	
34	1SG16EC024	17	20	20	19	18	18	19	18	
35	1SG16EC025	15	15	18	18	20	17	17	16	
36	1SG16EC026	20	18	20	20	20	19	20	20	
37	1SG16EC027	19	17	19	20	20	20	16	19	
38	1SG16EC029	18	19	18	20	20	16	19	19	

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Sl NO.	USN	15EC61	15EC62	15EC63	15EC64	15EC654	15EC663	15ECL67	15ECL68	STUDENT SIGNATURE
39	1SG16EC030	12	15	13	15	14	16	18	15	
40	1SG16EC031	15	15	17	19	20	18	18	18	
41	1SG16EC033	17	16	19	17	20	20	19	19	
42	1SG16EC034	17	16	18	19	20	20	18	19	
43	1SG16EC035	17	17	15	19	20	18	17	18	
44	1SG16EC036	17	16	17	17	20	19	19	18	
45	1SG16EC037	13	17	17	15	18	16	18	18	
46	1SG16EC038	15	15	19	17	20	19	18	15	
47	1SG16EC039	16	17	20	19	19	17	17	18	
48	1SG16EC040	17	16	20	20	20	20	20	18	
49	1SG16EC041	12	12	12	14	15	14	14	17	
50	1SG16EC042	15	16	19	20	20	18	16	16	
51	1SG16EC043	13	13	16	18	16	14	18	17	
52	1SG16EC044	14	13	16	12	18	15	15	15	
53	1SG16EC045	18	15	17	20	20	19	16	18	
54	1SG16EC047	18	18	20	20	20	19	19	18	
55	1SG16EC048	19	18	20	20	20	18	19	18	
56	1SG16EC049	18	15	17	20	20	19	19	18	
57	1SG16EC050	19	15	19	19	20	18	19	18	
58	1SG16EC051	17	16	19	20	20	20	18	19	
59	1SG16EC052	13	14	15	15	14	12	14	15	
60	1SG16EC053	12	14	13	12	15	16	17	18	
61	1SG16EC054	14	13	19	16	18	17	17	20	
62	1SG16EC055	16	14	15	19	20	18	19	18	
63	1SG16EC056	14	13	16	16	17	14	16	15	
64	1SG16EC057	20	19	20	20	19	20	16	20	
65	1SG16EC059	12	15	14	13	15	16	18	18	
66	1SG16EC060	12	15	18	16	17	17	17	16	
67	1SG16EC062	17	18	17	20	20	16	19	19	
68	1SG16EC063	12	16	19	16	19	16	18	14	
69	1SG16EC064	16	17	19	19	18	16	18	20	
70	1SG16EC065	19	18	19	18	20	19	20	17	
71	1SG16EC066	16	17	19	16	20	18	19	17	
72	1SG16EC068	14	17	16	18	19	18	18	16	
73	1SG16EC070	20	18	20	20	20	18	20	19	
74	1SG16EC071	16	17	19	18	20	19	14	17	
75	1SG16EC072	10	12	14	14	14	17	16	15	
76	1SG16EC073	19	18	20	20	20	20	19	20	
77	1SG16EC074	16	18	16	18	17	17	20	19	
78	1SG16EC075	15	14	13	13	18	16	19	19	
79	1SG16EC076	11	13	12	13	16	12	12	14	
80	1SG16EC077	12	13	12	17	13	12	12	16	
81	1SG16EC078	13	12	16	13	16	18	18	18	
82	1SG16EC080	15	16	14	15	16	16	18	15	
83	1SG16EC081	16	16	14	18	18	18	12	16	

Principal
Sapthagiri College of Engineering
Chikkasandra, Hesaraghatta Road,

Sl NO.	USN	15EC61	15EC62	15EC63	15EC64	15EC654	15EC663	15ECL67	15ECL68	STUDENT SIGNATURE
84	1SG16EC082	19	19	18	19	20	20	20	19	
85	1SG16EC084	13	13	16	16	18	17	20	15	
86	1SG16EC085	15	18	17	18	19	15	19	18	
87	1SG16EC088	17	17	19	19	20	19	19	18	
88	1SG16EC089	13	15	16	17	19	13	18	15	
89	1SG16EC090	13	14	15	16	18	18	19	17	
90	1SG16EC091	17	19	18	18	20	17	20	18	
91	1SG16EC093	17	18	19	20	20	20	20	17	
92	1SG16EC094	18	17	20	15	19	20	19	18	
93	1SG16EC095	12	14	12	12	15	15	18	13	
94	1SG16EC096	15	14	15	17	20	17	18	15	
95	1SG16EC097	15	15	20	16	20	17	19	17	
96	1SG16EC098	17	15	18	19	20	17	19	16	
97	1SG16EC099	18	19	20	18	20	20	20	18	
98	1SG16EC100	14	15	18	15	19	17	19	16	
99	1SG16EC101	18	17	19	18	17	19	20	19	
100	1SG16EC102	10	12	12	12	12	11	17	13	
101	1SG16EC103	12	12	12	12	13	12	18	13	
102	1SG16EC104	14	14	15	15	17	18	19	17	
103	1SG16EC105	12	14	14	17	19	15	17	15	
104	1SG16EC106	12	13	12	12	16	12	17	17	
105	1SG16EC107	18	16	16	14	15	18	17	17	
106	1SG16EC109	12	16	14	12	18	13	17	15	
107	1SG16EC111	18	16	17	19	20	19	19	16	
108	1SG16EC112	16	19	19	19	20	18	19	17	
109	1SG16EC113	16	16	19	17	19	20	20	15	
110	1SG16EC114	17	12	13	13	20	14	18	17	
111	1SG16EC115	17	20	19	19	20	18	19	20	
112	1SG16EC118	13	19	18	14	16	16	19	16	
113	1SG16EC119	12	16	18	16	18	12	15	13	
114	1SG16EC120	12	15	12	15	16	12	17	14	
115	1SG16EC122	13	16	16	16	17	16	18	18	
116	1SG16EC123	12	16	16	17	20	17	20	15	
117	1SG16EC124	14	15	18	17	18	19	20	15	
118	1SG16EC125	13	13	12	16	14	14	16	16	
119	1SG16EC126	15	18	18	17	19	14	19	15	
120	1SG16EC127	14	13	13	16	17	13	19	19	
121	1SG16EC129	16	17	15	14	17	17	20	15	
122	1SG16EC130	12	14	15	14	18	14	18	19	
123	1SG16EC131	12	12	14	12	14	14	18	13	
124	1SG16EC400	13	12	14	12	16	16	17	15	
125	1SG16EC407	14	12	14	14	13	14	17	15	
126	1SG16EC414	15	14	13	14	15	16	19	18	
127	1SG16EC419	14	12	17	20	18	19	19	18	
128	1SG16EC422	12	15	14	16	17	13	17	16	

Sl NO.	USN	15EC61	15EC62	15EC63	15EC64	15EC654	15EC663	15ECL67	15ECL68	STUDENT SIGNATURE
129	1SG16EC424	12	13	13	15	15	14	20	18	
130	1SG16EC427	14	15	18	19	19	19	19	19	
131	1SG16EC433	14	16	14	15	18	12	18	16	
132	1SG17EC400	12	14	14	17	17	17	18	16	
133	1SG17EC401	12	14	18	17	16	16	15	16	
134	1SG17EC407	10	12	12	12	14	12	19	15	
135	1SG17EC408	13	15	13	15	18	16	19	14	
136	1SG17EC409	12	12	12	15	14	13	18	18	
137	1SG17EC411	12	12	12	17	16	14	17	16	
138	1SG17EC412	12	12	13	14	15	15	18	13	
139	1SG17EC413	13	14	14	15	15	13	16	15	
140	1SG17EC414	14	15	18	18	18	18	17	15	
141	1SG17EC418	14	14	19	20	16	18	19	16	
142	1SG17EC419	12	12	12	16	14	14	18	13	
143	1SG17EC420	17	17	17	18	17	19	19	20	
144	1SG17EC422	12	14	16	17	17	18	19	20	
--x--	Faculty Signature									----xxxxxxx----

* - values are either optional subjects or the faculty has not yet entered the marks

HOD
Seal and Signature

Head of the Department
Electronics & Communication
Sapthagiri College of Engineering
Bangalore-560 057

PRINCIPAL
Seal and Signature

Principal
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Bangalore-560 057

Principal
Sapthagiri College of Engineering
Chikkasandra, Hesaraghatta Road,
Bangalore-560 057

Visvesvaraya Technological University

SAPTHAGIRI COLLEGE OF ENGINEERING BENGALURU

Branch : EC Scheme : 2015 Semester : 8

Sl NO.	USN	15EC81	15EC82	15EC834	15EC835	15EC84	15ECP85	15ECS86	STUDENT SIGNATURE
1	1SG13EC088	12	12	-	14	44	89	80	
2	1SG13EC131	14	14	-	17	47	90	85	
3	1SG14EC037	12	13	-	17	42	88	80	
4	1SG14EC118	13	12	-	17	42	85	73	
5	1SG15EC001	17	15	17	-	45	95	89	
6	1SG15EC002	2	03	-	03	30	80	0	
7	1SG15EC003	12	14	-	15	50	96	84	
8	1SG15EC006	16	15	-	18	46	90	84	
9	1SG15EC007	12	14	13	-	45	90	75	
10	1SG15EC008	14	18	-	18	49	95	95	
11	1SG15EC009	17	16	-	18	48	94	85	
12	1SG15EC010	12	13	-	12	44	90	70	
13	1SG15EC011	12	12	-	13	45	88	70	
14	1SG15EC012	15	16	17	-	46	90	90	
15	1SG15EC013	12	12	-	12	50	98	90	
16	1SG15EC014	13	12	-	12	44	88	75	
17	1SG15EC015	17	14	-	18	45	88	83	
18	1SG15EC016	12	14	-	14	45	88	81	
19	1SG15EC018	14	12	-	15	45	92	81	
20	1SG15EC019	14	14	-	17	48	90	84	
21	1SG15EC020	14	20	-	20	49	96	93	
22	1SG15EC021	12	14	-	16	39	88	89	
23	1SG15EC022	12	13	-	14	46	92	75	
24	1SG15EC023	19	20	19	-	49	96	95	
25	1SG15EC024	15	16	-	16	46	96	90	
26	1SG15EC026	15	20	-	20	47	96	87	
27	1SG15EC027	13	14	-	12	45	94	80	
28	1SG15EC028	16	17	-	18	48	95	92	
29	1SG15EC030	12	12	-	12	40	85	70	
30	1SG15EC032	18	18	-	20	45	90	84	
31	1SG15EC033	13	13	-	15	45	90	90	
32	1SG15EC034	17	17	-	17	44	90	89	
33	1SG15EC035	13	13	16	-	45	92	87	
34	1SG15EC036	13	14	13	-	40	88	77	
35	1SG15EC037	15	13	19	-	50	96	88	

Sl NO.	USN	15EC81	15EC82	15EC834	15EC835	15EC84	15ECP85	15ECS86	STUDENT SIGNATURE
36	1SG15EC038	13	14	20	-	47	97	95	
37	1SG15EC039	15	14	-	14	42	90	91	
38	1SG15EC041	12	14	18	-	47	90	83	
39	1SG15EC042	16	14	-	17	45	92	82	
40	1SG15EC044	14	20	-	20	47	96	88	
41	1SG15EC045	19	14	19	-	44	95	93	
42	1SG15EC046	19	18	-	16	42	92	86	
43	1SG15EC047	14	14	19	-	49	98	95	
44	1SG15EC048	13	12	-	12	42	90	84	
45	1SG15EC051	15	19	-	19	45	94	88	
46	1SG15EC052	13	12	-	13	44	92	83	
47	1SG15EC053	16	15	20	-	45	92	90	
48	1SG15EC054	13	14	-	18	50	96	85	
49	1SG15EC057	12	12	13	-	42	93	87	
50	1SG15EC059	20	19	20	-	50	98	94	
51	1SG15EC061	13	12	-	17	46	97	82	
52	1SG15EC062	15	14	-	15	46	90	81	
53	1SG15EC064	18	19	-	18	43	94	95	
54	1SG15EC065	19	20	-	20	48	95	89	
55	1SG15EC066	19	18	-	20	50	96	97	
56	1SG15EC067	15	14	-	17	45	95	86	
57	1SG15EC069	17	18	-	17	43	95	89	
58	1SG15EC070	19	18	-	20	47	95	95	
59	1SG15EC071	12	14	-	15	42	91	82	
60	1SG15EC072	18	16	-	17	47	92	84	
61	1SG15EC073	19	18	-	20	47	95	89	
62	1SG15EC074	13	14	-	14	46	97	89	
63	1SG15EC075	19	20	-	20	50	98	97	
64	1SG15EC076	13	12	-	14	44	90	89	
65	1SG15EC078	12	19	13	-	45	92	88	
66	1SG15EC079	12	13	15	-	44	90	87	
67	1SG15EC080	18	18	-	20	50	96	96	
68	1SG15EC081	18	17	-	20	47	95	92	
69	1SG15EC082	18	16	-	18	42	92	95	
70	1SG15EC083	18	17	-	18	49	97	95	
71	1SG15EC084	13	17	-	15	49	98	87	
72	1SG15EC085	19	18	-	20	49	97	89	
73	1SG15EC086	19	18	-	20	50	94	90	
74	1SG15EC087	19	19	-	18	47	96	95	
75	1SG15EC090	13	13	-	16	42	94	86	
76	1SG15EC091	18	16	-	16	43	97	86	
77	1SG15EC093	18	15	-	16	46	94	85	

Sl NO.	USN	15EC81	15EC82	15EC834	15EC835	15EC84	15ECP85	15ECS86	STUDENT SIGNATURE
78	1SG15EC094	16	18	-	18	42	93	80	
79	1SG15EC099	15	15	-	16	46	94	88	
80	1SG15EC101	14	13	-	15	49	94	80	
81	1SG15EC102	18	17	-	20	48	95	85	
82	1SG15EC104	12	13	12	-	35	88	83	
83	1SG15EC105	15	13	-	12	37	88	81	
84	1SG15EC107	15	18	-	16	49	94	88	
85	1SG15EC108	18	16	-	20	44	95	89	
86	1SG15EC110	16	14	-	18	43	88	84	
87	1SG15EC112	14	12	-	12	40	87	75	
88	1SG15EC113	12	12	-	14	44	89	82	
89	1SG15EC114	18	17	-	20	48	98	88	
90	1SG15EC116	15	16	-	15	46	97	83	
91	1SG15EC119	16	12	-	12	40	85	72	
92	1SG15EC120	14	16	13	-	44	85	65	
93	1SG15EC121	19	19	-	18	42	90	82	
94	1SG15EC122	12	14	-	15	40	88	72	
95	1SG15EC123	12	13	-	14	41	85	72	
96	1SG16EC401	16	14	15	-	43	88	81	
97	1SG16EC402	15	14	-	17	44	92	83	
98	1SG16EC403	13	12	-	19	42	88	81	
99	1SG16EC405	15	12	-	18	44	92	84	
100	1SG16EC406	12	14	-	14	42	85	82	
101	1SG16EC408	12	12	-	12	42	88	67	
102	1SG16EC410	19	15	-	18	47	92	84	
103	1SG16EC411	17	16	20	-	49	98	94	
104	1SG16EC412	16	15	-	12	42	90	82	
105	1SG16EC413	12	12	-	15	46	98	88	
106	1SG16EC415	14	13	-	12	43	88	82	
107	1SG16EC418	13	14	-	12	47	98	82	
108	1SG16EC420	18	17	-	18	44	93	81	
109	1SG16EC421	12	14	-	14	47	90	82	
110	1SG16EC425	13	14	-	12	46	93	86	
111	1SG16EC429	13	14	-	17	44	92	82	
112	1SG16EC430	13	16	-	15	46	92	84	
113	1SG16EC431	13	12	-	15	45	95	81	
--x--	Faculty Signature								----XXXXXXX----

* - values are either optional subjects or the faculty has not yet entered the marks

HOD

Seal and Signature

Head of the Department
Electronics & Communication
Sapthagiri College of Engineering
Bangalore-560 057

PRINCIPAL

Seal and Signature

Sapthagiri College of Engineering
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Sapthagiri College of Engineering
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Bangalore- 560 057

Visvesvaraya Technological University

SAPTHAGIRI COLLEGE OF ENGINEERING BENGALURU

Branch : EC Scheme : 2010 Semester : 5

Sl NO.	USN	10AL51	10EC52	10EC53	10EC54	10EC55	10EC56	10ECL57	10ECL58	STUDENT SIGNATURE
1	1SG15EC411	18	15	15	16	20	15	16	16	
--x--	Faculty Signature									----xxxxxxx----

* - values are either optional subjects or the faculty has not yet entered the marks

HOD
Seal and Signature

Head of the Department
Electronics & Communication
Sapthagiri College of Engineering
Bangalore-560 057

PRINCIPAL
Seal and Signature

Principal
Sapthagiri College of Engineering
Chikkasandra, Hesaraghatta Road,
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Principal
Sapthagiri College of Engineering
Chikkasandra, Hesaraghatta Road,
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Visvesvaraya Technological University

SAPTHAGIRI COLLEGE OF ENGINEERING BENGALURU

Branch : LVS Scheme : 2017 Semester : 4

Sl NO.	USN	17ECS422	17ELD41	17EVE43	STUDENT SIGNATURE
1	1SG17LVS01	20	20	43	
--x--	Faculty Signature				----xxxxxxx----

* - values are either optional subjects or the faculty has not yet entered the marks

HOD
Seal and Signature

Head of the Department
Electronics & Communication
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Bangalore-560 057

PRINCIPAL
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Principal
Sapthagiri College of Engineering
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Bangalore- 560 057

Principal
Sapthagiri College of Engineering
Chikkasandra, Hesaraghatta Road,
Bangalore- 560 057

14/10/2019

SAPTHAGIRI COLLEGE OF ENGINEERING

(Affiliated to VTU, Belagavi & Approved by AICTE, New Delhi)
#14/5, Chikkasandra, Hesaraghatta main road, Bengaluru-560057

F-EXM-09/R0

DEPARTMENT OF ELECTRONICS AND COMMUNCIATION

VTU Exam Result Analysis: June/July 2019 **(ARV)** [EVEN Semester 2018-19]

SEMESTER: **6** SECTION: '**A**' PASS = **77.02% (57/74)**

Sl No.	Subject code	Subject	Faculty	Student strength :74											% of Pass (WOR)	% of Pass (WR)
				Appeared	Passed	Failed	Absent	S+	S	A	B	C	D	E		
1	15EC61	Digital Communication	Vinay HC	74	62	12	NIL	1	2	2	10	16	9	12	82.11	83.78
2	15EC62	ARM Microcontroller	Agalya P	74	71	3	NIL	0	7	5	19	26	6	8	97.29	95.94
3	15EC63	VLSI design	Shobha H	74	72	2	NIL	0	4	11	16	22	10	9	98.64	97.29
4	15EC64	Computer Communication networks	T Yadav	74	74	0	NIL	0	3	10	17	29	4	8	100	100
5	15EC654	Digital switching systems	Suma V Shetty	74	73	1	NIL	2	8	26	21	9	7	0	100	98.64
6	15EC663	Digital system design using Verilog	Vani A	74	70	4	NIL	0	4	3	10	29	15	0	90.54	94.59
7	15ECL67	Embedded controllers lab	Agalya P/Karthik NC	74	71	3	NIL	20	37	6	5	3	0	0	98.64	95.94
8	15ECL68	Computer networks lab	Vinay HC /T Yadav	74	73	1	NIL	24	24	3	2	10	10	0	100	98.64

Vinay HC 17/10/19
Coordinator 17/10/19

17/10/2019
Head of the Department
Electronics & Communication
Sapthagiri College of Engineering
Bangalore-560 057.

Principal
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Chikkasandra, Hesaraghatta Road,
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Principal
Sapthagiri College of Engineering
Chikkasandra, Hesaraghatta Road,
Bangalore-560 057

SEMESTER: 6 SECTION: 'B' PASS = 79.41% (54/68)

Sl No.	Subject code	Subject	Faculty	Student strength: 68											% of Pass (WOR)	% of Pass (WR)
				Appeared	Passed	Failed	Absent	S+	S	A	B	C	D	E		
1	15EC61	Digital Communication	Sandhya Rani MH	68	60	8	NIL	0	2	7	12	18	4	12	91.17	88.23
2	15EC62	ARM Microcontroller	Agalya P	68	68	0	NIL	0	3	8	12	24	10	9	100	100
3	15EC63	VLSI design	Shobha H	67	66	1	1	0	2	9	18	20	7	8	97.01	98.50
4	15EC64	Computer Communication networks	T Yadav	68	66	2	NIL	0	1	11	29	15	7	1	100	97.05
5	15EC654	Digital switching systems	Suma V Shetty	68	68	0	NIL	1	11	20	20	9	4	0	98.52	100
6	15EC663	Digital system design using Verilog	Vani A	67	60	7	1	0	0	8	15	19	6	8	91.04	88.23
7	15ECL67	Embedded controllers lab	Shobha S/Preethi TS	68	65	3	NIL	19	31	4	7	4	0	0	98.52	95.58
8	15ECL68	Computer networks lab	Sudha MS/Vani V	68	68	0	NIL	17	24	13	3	7	4	0	100	100

Principal
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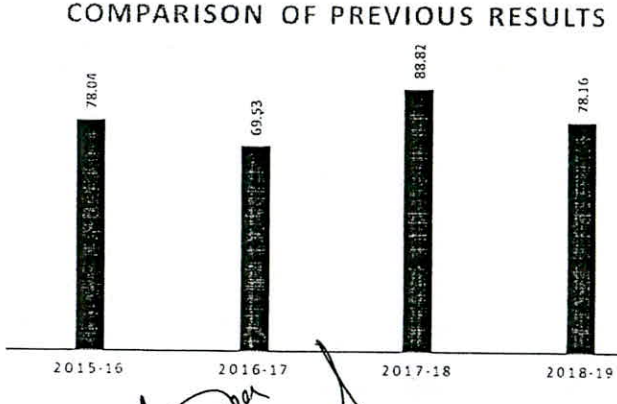
Bangalore-560 057

SEMESTER:6 SECTION: **'A & B'** (OVERALL) PASS =78.16% (111/142)

Sl No.	Subject code	Subject	Faculty	Student strength: 142											% of Pass (WOR)	% of Pass (WR)
				Appeared	Passed	Failed	Absent	S+	S	A	B	C	D	E		
1	15EC61	Digital Communication	Vinay HC/ Sandhya Rani MH	142	122	20	NIL	0	2	7	12	18	4	15	88.92	85.91
2	15EC62	ARM Microcontroller	Agalya P	142	139	3	NIL	0	3	8	12	24	10	10	97.88	97.88
3	15EC63	VLSI design	Shobha H	141	138	3	1	0	2	9	18	20	7	8	97.87	97.87
4	15EC64	Computer Communication networks	T Yadav	142	141	1	NIL	0	1	11	29	15	7	2	100	99.29
5	15EC654	Digital switching systems	Suma V Shetty	142	140	1	NIL	1	11	20	20	9	4	1	99.29	98.59
6	15EC663	Digital system design using Verilog	Vani A	141	130	11	1	0	0	8	15	19	6	8	90.84	92.19
7	15ECL67	Embedded controllers lab	Agalya P/Karthik NC Shobha S/Preethi TS	142	136	6	NIL	19	31	4	7	4	0	0	98.59	95.77
8	15ECL68	Computer networks lab	Vinay HC /T Yadav Sudha MS/Vani V	142	141	1	NIL	17	24	13	3	7	4	0	100	99.29



Comparison of previous results				
Academic year	2015-16	2016-17	2017-18	2018-19
Student appeared	123	128	111	142
Passed	96	89	98	98
Failed	27	39	13	44
Absent	0	0	0	0
Overall pass BRV %	70.00	61.71	84.68	69.01
Overall pass ARV %	78.04	69.53	88.82	78.16

Coordinator 17/6/19

Head of the Department
Electronics & Communication
Sapthagiri College of Engineering

Principal
Sapthagiri College of Engineering
Chikkasandra, Hesaraghatta Road,
Bangalore- 560 057

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Bangalore- 560 057

Fast Learners (Toppers)			
Sl. No	USN	NAME	Total Marks (Percentage)
1	1SG16EC023	DEEPIKA V	656
2	1SG16EC070	PAVITHRA R	652
3	1SG16EC073	PRAMILA K S	650
4	1SG16EC026	DIMPLE BHATT	646
5	1SG16EC112	SREEKEERTHI S	646
6	1SG16EC013	ASWINI D	642
7	1SG16EC099	SHOBHA M R	628
8	1SG16EC101	SHUBHAM JAISWAL	627
9	1SG16EC048	LAVANYA P	624
10	1SG16EC024	DEEPTHI M	619

Slow Learners			
Sl. No	USN	NAME	Total Marks (Percentage)
1	1SG15EC124	SHASHANK B.S.	371
2	1SG16EC400	ANUSHA R	361
3	1SG15EC060	MOHAMMED SHAHID	358
4	1SG15EC095	SANJAY KUMAR B N	351
5	1SG16EC015	BHOOMIKA N	345
6	1SG15EC117	MANU N M	344
7	1SG16EC102	SHUBHAM KHOSLA	333
8	1SG17EC407	HARSHINI P	331
9	1SG15EC100	SHASHIKANT KUMAR	311
10	1SG16EC422	SAMITHA M	268

17/10/19

Signature of Coordinator

HOD

Head of the Department
Electronics & Communication
Sapthagiri College of Engineering
Bangalore-560 057.

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