CBCS SCHEME

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15EC33

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define combinational logic. Design a combinational circuit which takes two, 2 bit binary numbers as its input and generates an output equal to 1, when the sum of the two numbers is even. **(10 Marks)**

b. Simplify using Karnaugh map. Write the Boolean equation and realize using NAND gates.
$D = f(w, x, y, z) = \Sigma m(0, 2, 4, 6, 8) + \Sigma d(10, 11, 12, 13, 14, 15)$. **(06 Marks)**

OR

2 a. Define canonical SOP and canonical POS. Expand $f = (\bar{a} + b + c)(a + c + \bar{d})$ into canonical POS. **(04 Marks)**

b. Solve using Quine-McCluskey tabulation method,
$f(a, b, c, d) = \Sigma m(0, 1, 4, 5, 9, 10, 12, 14, 15) + \Sigma\phi(2, 8, 13)$
Obtain the minimal form of the given function. Verify the result using k–map. **(12 Marks)**

Module-2

3 a. Define decoder. Implement full subtractor using a decodes. Write the truth table. **(08 Marks)**

b. Compare ripple carry adder and look ahead carry adder. Explain the circuit and operation of a 4 bit binary adder with look ahead carry. **(08 Marks)**

OR

4 a. Design and implement one bit comparator. **(04 Marks)**

b. Implement the multiple functions :
$f_1(a, b, c, d) = \Sigma(0, 4, 8, 10, 14, 15)$ and
$f_2(a, b, c, d) = \Sigma(3, 7, 9, 13)$
using two 3 to 8 decoders, i.e. 74138 ICs. **(06 Marks)**

c. Implement full adder circuit using 8 : 1 multiplexer. **(06 Marks)**

Module-3

5 a. What is gated SR Latch? Explain the operation of gated SR Latch, with a logic diagram, truth table and logic symbol. **(08 Marks)**

b. Derive the characteristic equation of SR, JK, D and T flip-flops with the help of function tables. **(08 Marks)**

OR

6 a. Explain the operation of a switch debouncer built using SR Latch. Draw the supporting waveforms. **(04 Marks)**

b. Explain 0s and 1s catching problem of Master Slave JK flip flop with waveform. Suggest the solution for this problem. **(04 Marks)**

c. What is edge triggered flip flop? With a neat circuit diagram, explain the operation of positive edge triggered D flip flop, using NAND gates. **(08 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain with illustration, a simple design methodology followed in IC industries. **(08 Marks)**

b. Explain the following constraints imposed in real world circuits :
i) Noise margin ii) propagation delay. **(03 Marks)**

c. Develop a verilog model for a 7–segment decoder, include an additional input, blank, that overrides the BCD i/p and causes all segments not to be lit. **(05 Marks)**

OR

2 a. Develop a verilog module of a debouncer for a push button switch that uses a debounce interval of 10ns. Assume the system clock frequency is 50 MHz. **(06 Marks)**

b. Design and develop a circuit and verilog module for modulo 10 counters. **(06 Marks)**

c. What is the distinction between a Moore and Mealy finite state machine? **(04 Marks)**

Module-2

3 a. Write a symbol for basic memory component and explain its parts. **(06 Marks)**

b. Explain about the multiport memories. **(06 Marks)**

c. Compute the 12-bit ECC word corresponding to the 8-bit data word "0110001". **(04 Marks)**

OR

4 a. Design a 64 K × 16 bit composite memory using 16K × 8 bit component. **(08 Marks)**

b. What is the difference between asynchronous static RAM and synchronous static RAM? **(06 Marks)**

c. Using a Hamming code, how many check bits are required for single error correction and double error detection for 4-bit data word? **(02 Marks)**

Module-3

5 a. Design a priority encoder that has 16 inputs, i[0 : 15]; a 4-bit encoded output, z[3 : 0] and a valid output ie. '1' when any input is '1'. Input i[0] has the highest priority and i[15] is the lowest priority. **(08 Marks)**

b. Explain the concept of differential signaling. How does differential signaling improve noise immunity? **(08 Marks)**

OR

6 a. What are the purpose of logic blocks and I/O blocks in FPGA? **(06 Marks)**

b. Explain different types of PCB design. **(03 Marks)**

c. Explain with a neat diagram of the internal organization of a CPLD. **(07 Marks)**

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USN | | | | | | | | | | 10EC61

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Communication

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions, selecting at least TWO questions from each part.***
2. ***Assume any missing data.***

PART – A

1 a. Show that time shifted Sinc function used in reconstruction of sampled signals i.e Sinc (2Wt – n) are mutually orthogonal. **(06 Marks)**

b. Explain the quadrature sampling with related block diagram, spectra and equations. **(06 Marks)**

c. A Signal g(t) consists of two frequency components f_1 = 3.9KHz and f_z = 4.1 KHz in such a relationship that they just cancel each other g(t) is sampled at the instants t = 0, T, 2T, ...

Where T = 125μs. The signal g(t) is defined by $g(t) = \text{Cos}\left(2\pi f_1 t + \frac{\pi}{2}\right) + A\ \text{Cos}\ (2\pi f_2 t + \phi)$

Find the values of amplitude A and ϕ of the second frequency component. **(08 Marks)**

2 a. Explain TDM technique with a neat block diagram and relevant waveforms. **(06 Marks)**

b. The information in an analog signal voltage waveform is to be transmitted over a PCM system with an accuracy of ± 0.1% (full scale)

The analog voltage waveform has a bandwidth of 100Hz and an amplitude range of -10 to +10 volts.

i) Determine the maximum sampling rate required
ii) Determine the number of bits in each PCM word
iii) Determine the minimum bit rate required in the PCM signal
iv) Determine the minimum absolute channel bandwidth required for the transmission of the PCM signal. **(08 Marks)**

c. What is the need for non-uniform quantization? Explain μ-law companding. **(06 Marks)**

3 a. With the block diagrams, explain the Adaptive delta modulation system. **(07 Marks)**

b. A Delta modulation system is tested with a 10-KHz Sinusoidal signal with 1V peak to peak at the input. It is sampled at 10 times the Nyquist rate

i) What is the step size required to prevent slope over load?
ii) What is the corresponding SNR? **(07 Marks)**

c. Present the data 100111010 using the following digital data formats.
i) Unipolar RZ ii) Split phase Manchester ii) M-ary system where m = 4. **(06 Marks)**

4 a. Define intersymbol interference and explain ideal solution for zero ISI with a mathematical scheme. **(08 Marks)**

b. A binary PAM wave is to be transmitted over a low-pass channel with an absolute maximum bandwidth of 75KHz. The bit duration is 10μSec. Find the raised Consine spectrum that satisfies these requirements. **(06 Marks)**

c. Write a note on Adaptive equalization. **(06 Marks)**

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Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
ARM Microcontroller and Embedded Systems

Time: 3 hrs.   Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain architectural features of cortex M3 with block diagram. **(07 Marks)**
b. Briefly describe the special registers of cortex M3. **(06 Marks)**
c. What is stack and what are the instructions to access stack? **(03 Marks)**

OR

2 a. Briefly discuss features of built in nested vector interrupt controller. **(08 Marks)**
b. Write a short note on :
i) Debugging support
ii) Interrupts and exceptions supported by cortex M3. **(08 Marks)**

Module-2

3 a. Explain memory map of cortex M3 with diagram. **(08 Marks)**
b. Write C language program to toggle an LED with small delay in cortex M3. **(05 Marks)**
c. Explain the 32 bit multiply instruction set. **(03 Marks)**

OR

4 a. Explain arithmetic instruction set with example. **(07 Marks)**
b. Briefly explain shift and rotate instructions with diagrams. **(07 Marks)**
c. Explain working of following instructions :
i) CMP ii) TST iii) CMN iv) REV. **(02 Marks)**

Module-3

5 a. Explain the sequence of operations for communicating with an I2C slave device. **(08 Marks)**
b. Write the differences between :
i) RISC and CISC
ii) Harvard architecture and Von Neumann architecture. **(08 Marks)**

OR

6 a. Briefly explain PLDs and types of PLDs. **(06 Marks)**
b. Write short note on :
i) Optocoupler
ii) COTS. **(08 Marks)**
c. Explain working of DRAM. **(02 Marks)**

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10EC662

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Satellite Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Describe the characteristics of the domestic satellites which provides a DTH television services. **(08 Marks)**

b. With neat sketch, explain the principle of operation and its features of polar orbiting satellites and its applications. **(07 Marks)**

c. Explain the services offered by INTELSATs. **(05 Marks)**

2 a. State Kepplers 3 laws of planetary motion. Illustrate in each case their relevance to artificial satellites orbiting the earth. **(08 Marks)**

b. What are the conditions to be satisfied for an orbit to be geo stationary and the information needed to determine the look angles for a geo stationary orbit. **(07 Marks)**

c. A geo stationary satellite is located at 85°W, calculate the azimuth angle for an ES antenna at lat 30°N and long 98°W. Calculate elevation angle, sketch the azimuth angle related to the angle A. **(05 Marks)**

3 a. Calculate for a free of 12 GHz, el = 22° for the horizontal polarization used for the rain rate $R_{0.01}$ = 15mm/h, h_0 = 600m and h_R = 1500m. Calculate the rain attenuation. Give a_h = 0.0188 and b_h = 1.217. **(05 Marks)**

b. Derive a suitable expression for $[CNR]_U$ and $[CNR]_D$ for a link budget calculation. **(07 Marks)**

c. Discuss various space link design transmission losses. **(08 Marks)**

4 a. Briefly describe various units of transponder for a C band communication satellite, construct a wide band receiver. Discuss how the capacity of a transponder can be increased. **(08 Marks)**

b. Describe various methods used for attitude control. **(06 Marks)**

c. With neat block diagram explain the role of TT and C. **(06 Marks)**

PART – B

5 a. Explain the role of indoor and outdoor unit in earth segment with neat block diagram explain the home terminal for DBS TV/FM reception. **(10 Marks)**

b. With neat sketches explain the basic blocks of transmit receive earth station. **(10 Marks)**

6 a. EIRP from Sat_1 is 30 dBW, G_R is 44 dB in desired direction and 25.67dB towards interfering satellite. The interfering satellite also radiates an EIRP of 34dBW. The polarization discrimination is 4dB. EIRP from ES is 24 dBW, ANT gain is 55dB and neigbhour sat. txit at 30 dBW. The off axis gain in the S_{at_1} direction is 25.67 dB. Polarization discrimination is 4 dB. Calculate $\left[\frac{C}{I}\right]_{ant}$. **(04 Marks)**

b. Illustrate basic TDMA concept. Explain the basic equipment block of TDMA and frame and burst formats for a TDMA system. **(08 Marks)**

c. With neat sketch, explain the principle of operation of channel assignment of a transponder and its traffic for a preassigned FDMA system. **(08 Marks)**