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**SAPTHAGIRI COLLEGE OF ENGINEERING**
**Department of Electronics and Communication**
**Internal Assessment –I/II/III**

Subject: VLSI DESIGN — Sub Code:15EC63

Semester/Section:VI(A&B) — Max Marks: 30

Duration: 1.5 hours — Date:23-03-18

Note: **Answer any two full questions, choosing one from each module**

| Question No. | Questions | Marks | BLT | CO's |
|---|---|---|---|---|
| | **Module-1** | | | |
| 1 a. | Explain with neat sketches N well CMOS fabrication | 07 | L2 | CO1 |
| b. | Draw CMOS Inverter using P –well. | 03 | L2 | CO1 |
| c. | Explain operating modes in MOS Transistor. | 05 | L2 | CO1 |
| | **OR** | | | |
| 2 a. | Discuss DC transfer characteristics of CMOS Inverter with relevant expressions. | 10 | L2 | CO1 |
| b. | Explain Latch up condition in CMOS with neat fig. | 05 | L2 | CO1 |
| | **Module-2** | | | |
| 3 a. | Discuss different static load Inverters with neat figs | 05 | L2 | CO1 |
| b. | Write CMOS LOGIC structure for given Boolean expression Y= ABC+BD+EF. | 05 | L1,L3 | CO2 |
| c. | List different layers of MOS transistors with color code and stick encoding. | 05 | L2 | CO2 |
| | **OR** | | | |
| 4 a. | Write stick diagram and layout for 2 inputs NAND gate | 08 | L1,L3 | CO2 |
| b. | Explain operation of BiCMOS Inverter. | 07 | L2 | CO2 |

COs:

**CO1:** Demonstrate MOS transistor theory, CMOS fabrication flow

**CO2:** Draw stick diagram and layout for logic gates with knowledge of physical design aspects.

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**SAPTHAGIRI COLLEGE OF ENGINEERING**
**Department of Electronics and Communication**
**Internal Assessment –II**

Subject: VLSI DESIGN
Semester/Section:VI(A&B)
Duration: 1.5 hours

Sub Code:15EC63
Max Marks: 30
Date: 18/04/18

Note: **Answer any two full questions, choosing one from each module**

| Question No. | Questions | Marks | BLT | CO's |
|---|---|---|---|---|
| | **Module-1I** | | | |
| 1 a. | What are scaling factors for i)Gate Capacitance ii)Max Operating Frequency iii)Current Density iv)Gate Delay v)Power Dissipation. | 05 | L1 | CO2 |
| b. | Define Sheet Resistance and Standard unit of Capacitance.Calculate on resistance for NMOS Inverter with $R_s$ =10Kohms $Z_{PU}$: $Z_{PD}$ ratio as 4:1,v=5v and Calculate power dissipation. | 05 | L1,L3 | CO2 |
| c. | Discuss the following in scaling of MOS CIRCUITS i)Limits of miniaturization ii) Limite of Interconnect and contact Resistance. | 05 | L6 | CO2 |
| | **OR** | | | |
| 2 a. | Derive the equation for Rise Time and Fall Time for CMOS Inverter. | 10 | L3 | CO2 |
| b. | What are the properties of NMOS and PMOS switches.How Transmission gate is usefull. | 05 | L1,L4 | CO2 |
| | **Module-III** | | | |
| 3 a. | What are general considerations to be followed in designing a subsystem. | 05 | L1 | CO3 |
| b. | What are basic requirements of shifter.?Explain with an example 4*4 cross bar switch.What are limitations of this and how it is overcome? | 10 | L1,L2 | CO3 |
| | **OR** | | | |
| 4 a. | What are guidelines for good VLSI design and problem associated with VLSI design. | 05 | L1 | CO3 |
| b. | Explain design steps for 4 bit Adder. | 10 | L2 | CO3 |

COs:CO1: Deriving Scaling Models for MOS Devices.

CO3: Designing Subsystems.

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| USN | 1 | S | G | 1 | 5 | E | C | | | |
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# SAPTHAGIRI COLLEGE OF ENGINEERING
## Department of Electronics and Communication
## Internal Assessment –III

**Subject: VLSI DESIGN** | **Sub Code:15EC63**
**Semester/Section: VI(A&B)** | **Max Marks: 30**
**Duration: 1.5 hours** | **Date:15/05/2018**

Note: **Answer any two full questions, choosing one from each module**

| Question No. | Questions | Marks | BLT | CO's |
|---|---|---|---|---|
| | **Module-V** | | | |
| 1 a. | Explain timing considerations of memory elements. | 05 | L2 | CO4 |
| b. | Define two phase clock. | 02 | L1 | CO4 |
| c. | Explain Pseudo static Memory element with neat figure. | 08 | L2 | CO4 |
| | **OR** | | | |
| 2 a. | Explain 3 transistor dynamic memory cell. | 10 | L2 | CO4 |
| b. | Explain 1T dynamic cell with neat figure. | 05 | L2 | CO4 |
| | **Module-IV** | | | |
| 3 a. | Discuss structured design approach for 4 bit Parity generator. | 05 | L6 | CO4 |
| b. | Write schematic and stick diagram for 4:1 Multiplexer. | 05 | L1 | CO4 |
| c | Design 4 bit Gray to Binary convertor. | 05 | L6 | |
| | **OR** | | | |
| 4 a. | Discuss different Bus architectures with neat sketches. | 10 | L6 | CO4 |
| b. | Explain operation of 4 bit Dynamic shift Register with an example. | 05 | L2 | CO4 |

COs: CO4 Designing Of various Subsystems and issues related to designing.

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USN | | | | | | | | | |

# SAPTHAGIRI COLLEGE OF ENGINEERING, BENGALURU-560057
## DEPARTMENT OF ELECTRONICS AND COMMUNICATION
## INTERNAL ASSESSMENT – I

**Subject: Micro processors** **Sub Code: 15EC42**
**Semester/Section: 4th 'A' & 'B'** **Max Marks: 30**
**Duration: 1.5 hrs.** **Date: 23/03/2018**

**Note: Answer any two full questions, choosing one from each module**

| Question No. | Questions | Marks | BLT | CO's |
|---|---|---|---|---|
| | **Module-1** | | | |
| 1 a. | Explain the internal architecture of 8086 with its neat block diagram. | 08 | L2 | CO1 |
| b. | Explain briefly any five addressing modes of 8086 with an example for each. | 07 | L2 | CO1 |
| 2 a. | Explain the function of 8086 flags register. | 07 | L2 | CO1 |
| b. | If CS=5000H, DS=75A0H, SS=9210H, ES=A890H, BX=70A5H, BP=3575H, find the physical address of the source data for the following instructions MOV DL,[BX+5000H] SUB CH,[BP+7] CMP AX,[1000H] | 06 | L3 | CO1 |
| c. | Identify the addressing modes of the following instructions: ADD AX,[SI] MOV CL,[5000] MOV 25[BX+SI] SUB CX,5 | 02 | L3 | CO1 |
| | **Module-2** | | | |
| 3 a. | Explain the function of AAA, IDIV, CMPS instructions with an example for each. | 09 | L2 | CO1 |
| b. | Illustrate logical shift instructions of 8086 with an example for each. | 06 | L2 | CO1 |
| 4 a. | Develop an ALP to exchange two blocks within the memory. Consider five words in each block. | 06 | L3 | CO2 |
| b. | Develop an ALP to add 12345678H and 9ABCDEF0H. The result has to be stored in the memory. | 05 | L3 | CO2 |
| c. | Identify the errors in the following instructions and make the corrections. MOV DS,1234H MOV ES,DS SUB [5000H],[9000H] | 04 | L3 | CO2 |

**CO : Course Outcome CO1:** The students will be able to explain the architecture of 8086 microprocessor and its addressing modes.**CO2:** The students will be able to develop assembly level language program using the 8086 instruction set.

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**SAPTHAGIRI COLLEGE OF ENGINEERING, BENGALURU-560057**
**DEPARTMENT OF ELECTRONICS AND COMMUNICATION**
**INTERNAL ASSESSMENT –II**

**Subject: Microprocessors** **Sub Code: 15EC42**
**Semester/Section: 4th 'A' & 'B'** **Max Marks: 30**
**Duration: 1.5Hrs.** **Date: 18/04/2018**

**Note: Answer any two full questions, choosing one from each module**

| Question No. | Questions | Marks | BLT | CO's |
|---|---|---|---|---|
| | **Module-2** | | | |
| 1 a. | Develop an assembly level language program to identify smallest number in the given set of numbers:5F2CH, C11DH, 922AH, ABCEH, FFFFH, 9876H, 6789H, 1235H, FEEDH, 9FCDH. Store the result in the memory. | 08 | L3 | CO2 |
| b. | Develop an assembly level language program to count odd numbers from the given set of numbers:5F2CH, C11DH, 922AH, ABCEH, FFFFH, 9876H, 6789H, 1235H, FEEDH, 9FCDH. Store the count value in DH register. | 07 | L3 | CO2 |
| | | | | |
| 2 a. | Develop an assembly level language program to check whether the 16 bit number 3333H is even or odd parity. | 05 | L3 | CO2 |
| b. | Develop an assembly level language program to check whether the 16 bit number C3C3H is bitwise palindrome or not. | 05 | L3 | CO2 |
| c. | Develop an assembly level language program to check whether the character 'I' is a part of the string "WE SHOULD FOLLOW THE TRAFFIC RULES ". | 05 | L3 | CO2 |

| Question No. | Questions | Marks | BLT | CO's |
|---|---|---|---|---|
| | **Module-3** | | | |
| 3 a. | Explain the stack structure of 8086 and the operations of PUSH, POP instructions. | 09 | L2 | CO3 |
| b. | Develop an assembly level language program to find the factorial of an eight bit number and factorial value is of maximum eight bit. Make use of procedure while developing the given program. | 06 | L3 | CO3 |
| | | | | |
| 4 a. | What is interrupt in 8086? Briefly discuss about sequence of steps which occurs after executing INTR and IRET instruction in 8086. | 06 | L1 | CO3 |
| b. | Explain Type0, Type1, Type2, Type3,Type4 interrupts of 8086. | 09 | L2 | CO3 |

**BLT**: Bloom's Taxonomy
**CO:** Course Outcome
**CO2:** Able to develop assembly level language program using the 8086 instruction set.
**CO3:** Able to explain the stack structure, Interrupts and its usage in the program.

**-----ALL THE BEST-----**

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**SAPTHAGIRI COLLEGE OF ENGINEERING, BENGALURU-560057**
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**INTERNAL ASSESSMENT –III**

**Subject: Microprocessors** **Sub Code: 15EC42**
**Semester/Section: 4th 'A' & 'B'** **Max Marks: 30**
**Duration: 1.5Hrs.** **Date: 15/05/2018**

**Note: Answer any two full questions, choosing one from each module**

| Question No. | Questions | Marks | BLT | CO's |
|---|---|---|---|---|
| | **Module-4** | | | |
| 1 a. | Briefly explain the signals ALE, $\overline{INTA}$, $\overline{TEST}$, READY, RESET. | 07 | L2 | CO4 |
| b. | Explain the operation of 8086 in minimum mode with the help of block diagram and timing diagrams. | 08 | L2 | CO4 |
| | | | | |
| 2 a. | Summarize special processor activities in 8086. | 07 | L2 | CO5 |
| b. | It is required to interface two chips of 32K X 8 ROM and four chips of 32K X 8 RAM with 8086, according to the following map:<br>ROM 1 and 2 F0000H to FFFFFH, RAM 1 and 2 D0000H to DFFFFH<br>RAM 3 and 4 E0000H to EFFFFH. Construct the memory system according to the given map. | 08 | L3 | CO5 |

| Question No. | Questions | Marks | BLT | CO's |
|---|---|---|---|---|
| | **Module-5** | | | |
| 3 a. | Explain the physical memory organization of 8086. | 07 | L2 | CO4 |
| b. | Explain the operation of 8086 in maximum mode with the help of block diagram and timing diagrams. | 08 | L2 | CO4 |
| | | | | |
| 4 a. | Construct a system by interfacing DAC0800 to 8086 using 8255 and develop an assembly language program to generate a triangular wave of frequency 500Hz. The amplitude of the triangular wave should be +5V.The 8086 operates at 8MHz. | 07 | L3 | CO5 |
| b. | Construct a system by interfacing a stepper motor to 8086 using 8255 and develop a program to rotate the motor shaft in clockwise direction 5 steps or counter clockwise direction 10 steps depending upon the content of memory location 2000H is 0 or FFH respectively. | 08 | L3 | CO5 |

LT: Bloom's Taxonomy
O: Course Outcome
O4: Able to explain the operation of 8086 in minimum mode as well as maximum mode.
O5: Able to interface 8086 with peripheral devices.

-----ALL THE BEST-----

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